Desemicore

D8820

20V Dual N-Channel Enhancement Mode MOSFET

■ DESCRIPTION

The 8820 is the Dual N-Channel logic enhancement mode power field effect transistor which is produced using high cell density advanced trench technology to provide excellent $R_{DS(ON)}$.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-lin power loss are needed in a very small outline surface mount package

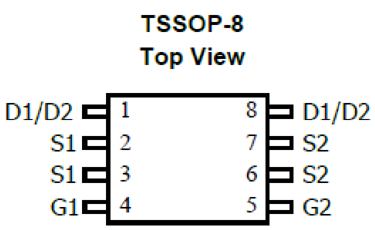
■ FEATURE

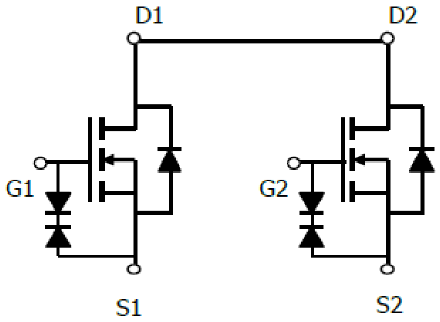
- ***20V/7.5A, $R_{DS(ON)}$=16.5mΩ(typ.) @V_{GS}=4.5V***
- ***20V/5.5A, $R_{DS(ON)}$=25mΩ(typ.) @V_{GS}=2.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- This is a Full RoHS compliance
- ESD Rating:2000V HBM
- TSSOP8 package design

■ APPLICATIONS

- Power Management in Note Book
- Portable Equipment
- Battery Powered System

■ PIN CONFIGURATION





■ PART NUMBER INFORMATION

8820A-BB C	A=Package Code T: TSSOP8 BB=Handing Code TR: Tape&Reel C=Lead Plating Code G: Green Product

■ ORDERING INFROMATION

Part Number	Package Code	Package	Shipping
8820T-TR	T	TSSOP8	3000EA / T&R

※ Year Code : 0~9

※ Week Code : A~Z(1-26)

※ G : Green Product. This product is RoHS compliant.

■ ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Continuous Drain Current (T_A=25℃)	V_{GS}=10V	7.0	A
	Continuous Drain Current (T_A=75℃)		6.0	A
I_{DM}	Pulsed Drain Current		30	A
I_S	Continuous Source Current (Diode Conduction)		1	A
P_D	Power Dissipation	T_A=25℃	1.5	W
		T_A=75℃	1.0	
T_J	Operation Junction Temperature		150	℃
T_{STG}	Storage Temperature Range		-55~+150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ THERMAL DATA

Symbol	Parameter	Min	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		62.5		℃/W

■ *ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	0.4	0.6	1.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±10V			±10	uA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=16V, V_{GS}=0			1	uA
		V_{DS}=16V, V_{GS}=0 T_J=55℃			5	
$I_{D(ON)}$	On=State Drain Current	V_{DS}≧5V, V_{GS}=4.5V	7.5			A
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=7.5A	14	16	18	mΩ
		V_{GS}=4.5V, I_D=7A	14	18.5	22	
		V_{GS}=3.6V, I_D=6.5A	16	20	24	
		V_{GS}=2.5V, I_D=5.5A	18	25	30	
		V_{GS}=1.8V, I_D=5A	20	24	34	
G_{fs}	Forward Transconductance	V_{DS}=5V, I_D=7A		31		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=1.0A, V_{GS}=0V		0.7	1.3	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=10V V_{GS}=4.5V I_D=7.0A		16		nC
Q_{gs}	Gate-Source Charge			1.7		
Q_{gd}	Gate-Drain Charge			6.8		
C_{iss}	Input Capacitance	V_{DS}=10V V_{GS}=0V f=1MHz		1120		pF
C_{oss}	Output Capacitance			1950		
C_{rss}	Reverse Transfer Capacitance			155		
$T_{d(on)}$	Turn-On Time	V_{DS}=10V I_D=7.0A V_{GEN}=5V R_G=3.3Ω		7.2		nS
T_r				11		
$T_{d(off)}$	Turn-Off Time			64		
T_f				32		

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

2.Static parameters are based on package level with recommended wire bonding

■ *TYPICAL CHARACTERISTICS (25℃ Unless Note)*

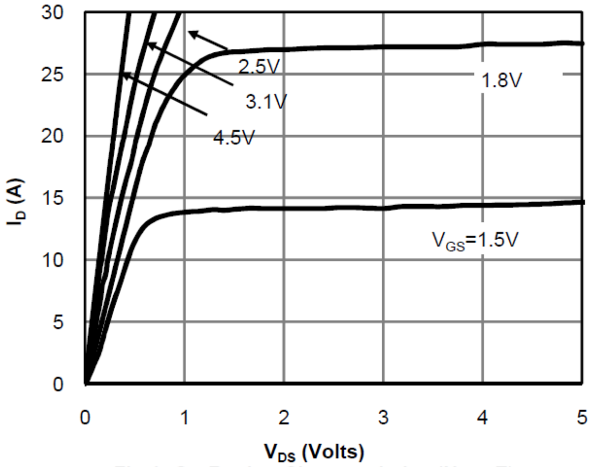


Fig 1: On-Region Characteristics (Note E)

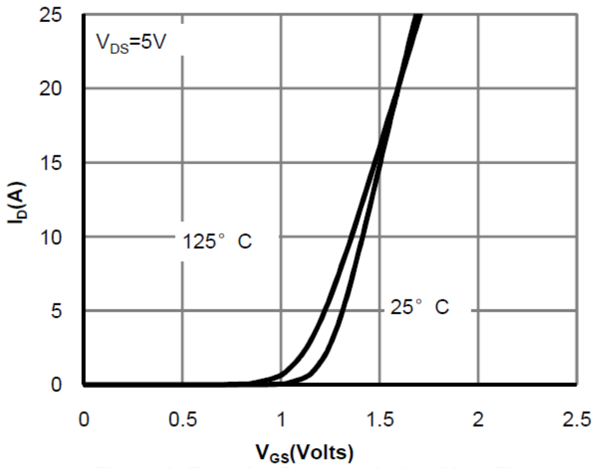


Figure 2: Transfer Characteristics (Note E)

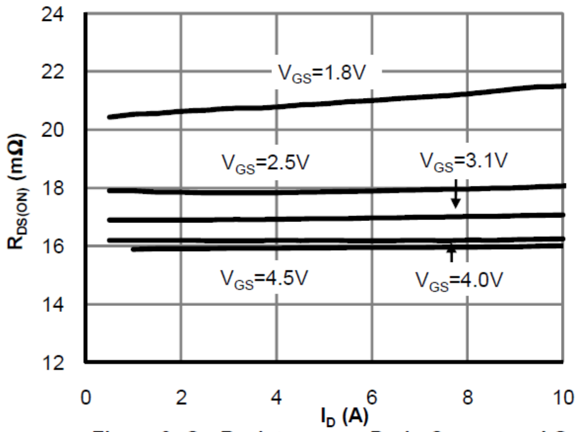


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

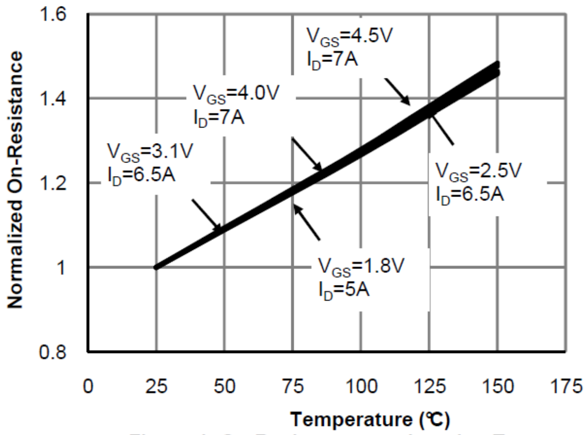


Figure 4: On-Resistance vs. Junction Temperature (Note E)

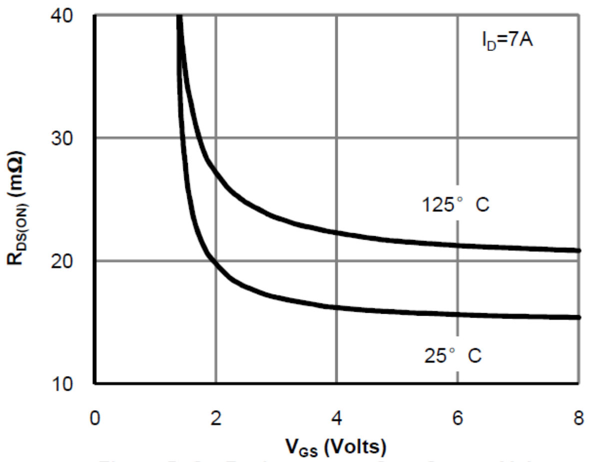


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

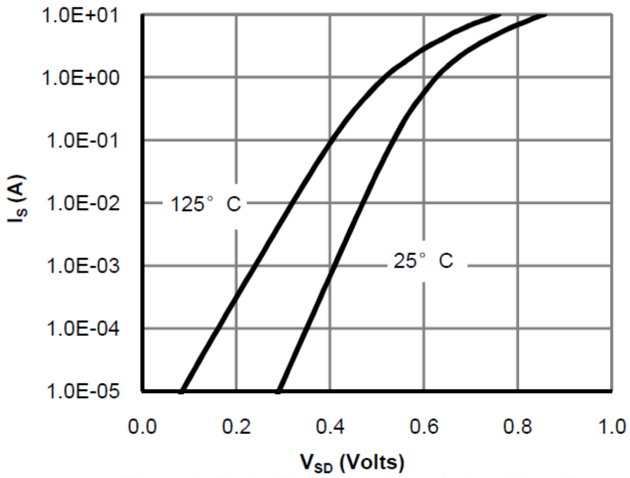


Figure 6: Body-Diode Characteristics (Note E)

■ *TYPICAL CHARACTERISTICS (continuous)*

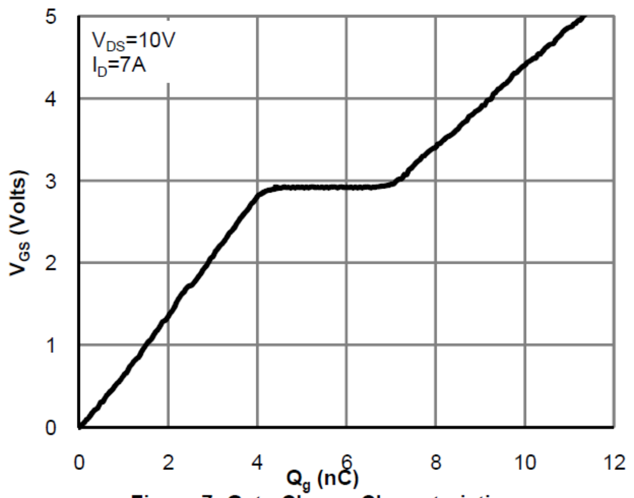


Figure 7: Gate-Charge Characteristics

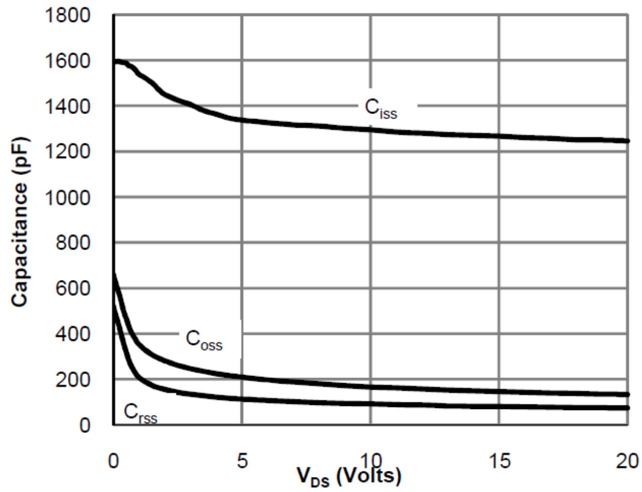


Figure 8: Capacitance Characteristics

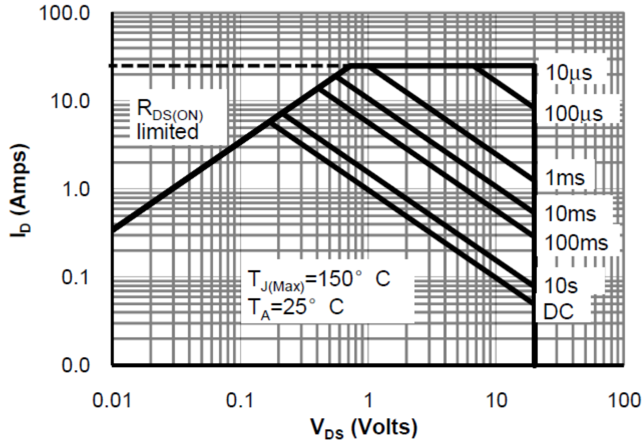


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

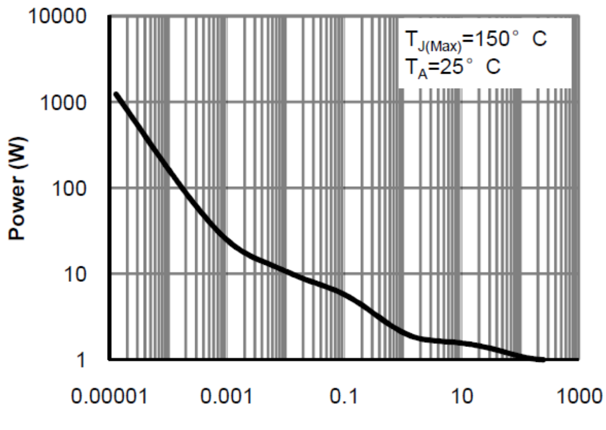


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

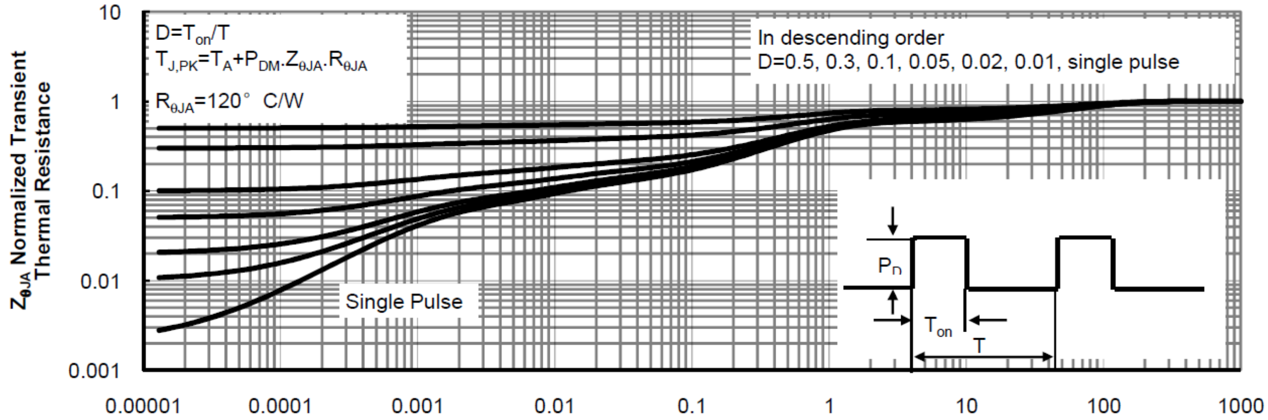
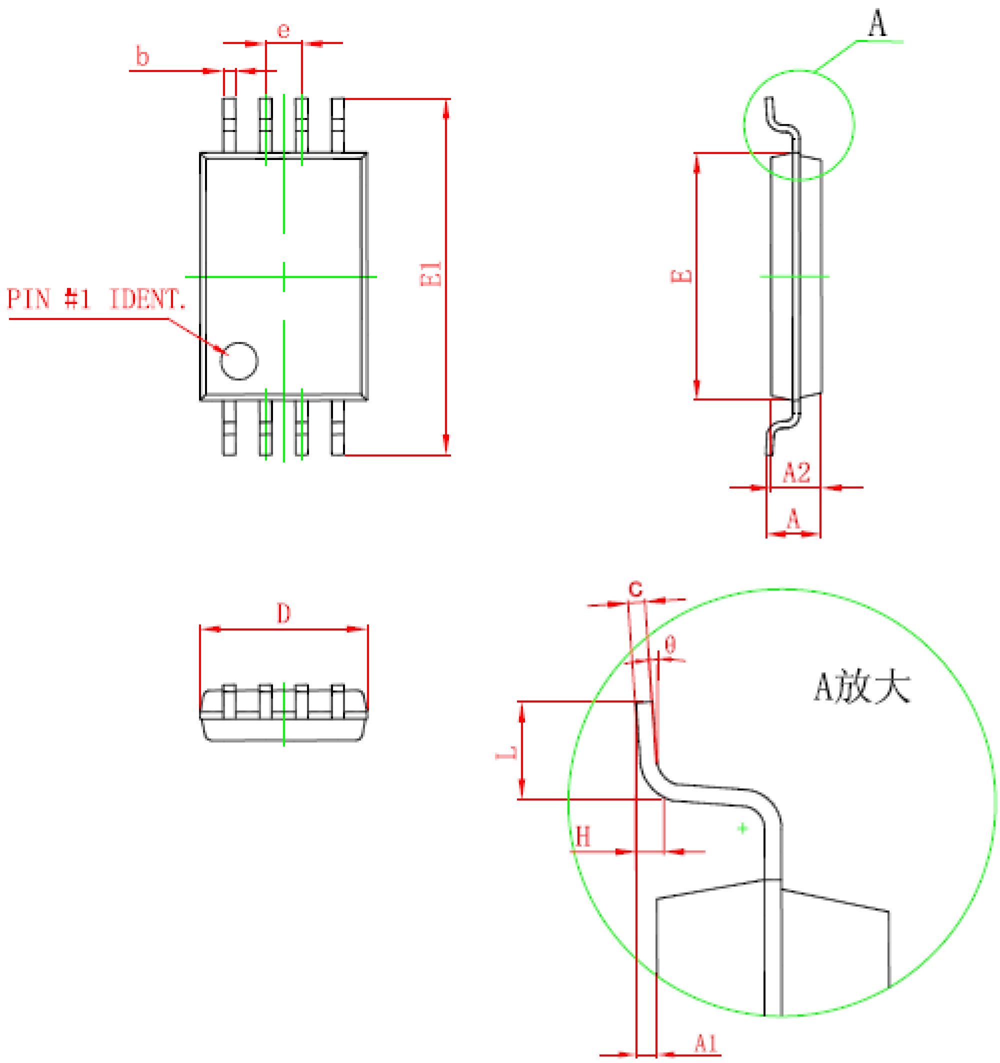


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TSSOP8L PACKAGE OUTLINE DIMENSIONS

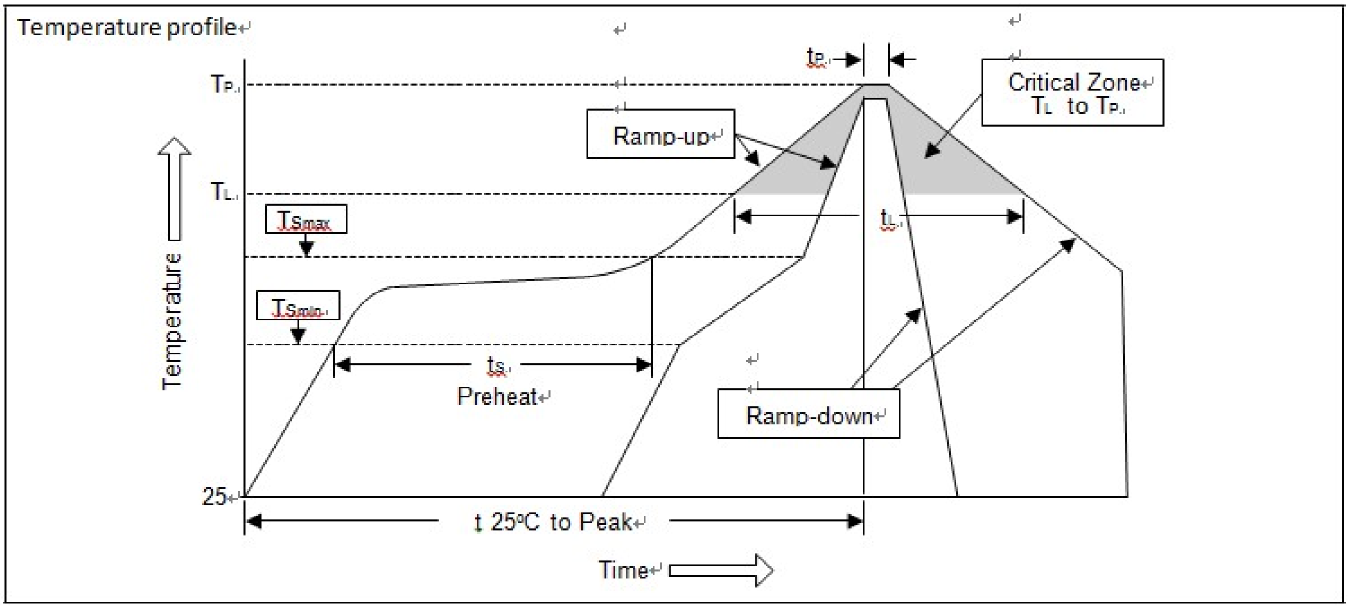


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

■ *SOLDERING METHODS FOR UNIVERCHIP*

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3℃/sec	<3℃/sec
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	 100℃ 150℃ 60~120 sec	 150℃ 200℃ 60~180 sec
Tsmax to T_L -Ramp-up Rate	<3℃/sec	<3℃/sec
Time maintained above -Temperature (T_L) -Time (t_L)	 183℃ 60~150 sec	 217℃ 60~150 sec
Peak Temperature (T_P)	240℃+0/-5℃	260℃+0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6℃/sec	<6℃/sec
Time 25℃ to Peak Temperature	<6 minutes	<6 minutes

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.