-20V P-Channel Enhancement Mode MOSFET

■ DESCRIPTION

The 7423 is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching

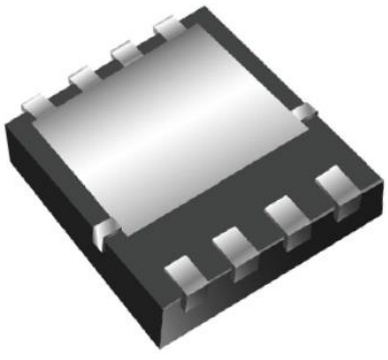
■ FEATURE

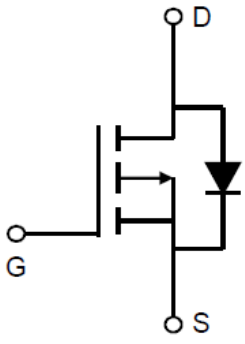
- ***-20V/-20A, $R_{DS(ON)}$=5mΩ (typ.)@V_{GS}=-4.5V***
- ***-20V/-20A, $R_{DS(ON)}$=7mΩ (typ.)@V_{GS}=-2.5V***
- ***I_D (at VGS=4.5V) = 50A***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- DFN3.3X3.3 EP-8L package design

■ APPLICATIONS

- High Frequency Point-of-Load Synchronous
- Newworking DC-DC Power System
- Load Switch

■ PIN CONFIGURATION





■ PART NUMBER INFORMATION

7423A-BB C	A= Package Code N: DFN BB=Handing Code TR: Tape&Reel C=Lead Plating Code G: Green Product

■ *ORDERING INFROMATION*

Part Number	Package Code	Package	Shipping
7423S-TRG	N	DFN3.3X3.3-EP8L	3000EA / T&R

※ Year Code : 0~9

※ Week Code : A~Z(1-26); a~z(27~52)

※ G : Green Product. This product is RoHS compliant.

■ *ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)*

Symbol	Parameter		Maximum	Unit
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Continuous Drain Current	T_c=25℃	-50	A
		T_c=100℃	-39	
I_{DM}	Pulsed Drain Current		-180	
I_{DSM}	Continuous Drain Current	T_A=25℃	-30	
		T_A=70℃	-24	
I_{AS}	Avalanche Current		-48	A
E_{AS}	Avalanche energy L=0.1mH		120	mJ
P_D	Power Dissipation	T_c=25℃	83	W
		T_c=100℃	33	
P_{DSM}	Power Dissipation	T_A=25℃	6.2	W
		T_A=70℃	4	
T_J	Operation Junction Temperature		150	℃
T_{STG}	Storage Temperature Range		-55~+150	℃
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		85	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ *ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-0.3	-0.4	-0.9	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±8V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-20V, V_{GS}=0			-1	uA
		V_{DS}=-20V, V_{GS}=0 T_J=55℃			-5	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-20A		5	6	mΩ
		V_{GS}=-2.5V, I_D=-20A		7	9	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=-1.0A, V_{GS}=0V		-0.71	-1.0	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=-10V		45	65	nC
Q_{gs}	Gate-Source Charge	V_{GS}=-4.5V		6.7		
Q_{gd}	Gate-Drain Charge	I_D=-15A		13		
C_{iss}	Input Capacitance	V_{DS}=-10V		4570		pF
C_{oss}	Output Capacitance	V_{GS}=0V		827		
C_{rss}	Reverse Transfer Capacitance	f=1MHz		565		
$T_{d(on)}$	Turn-On Time	V_{DS}=-10V		7		nS
T_r		I_D=-10A		12		
$T_{d(off)}$	Turn-Off Time	V_{GEN}=-10V		123		
T_f		R_G=3Ω		45		

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

2.Static parameters are based on package level with recommended wire bonding

■ *TYPICAL CHARACTERISTICS (25℃ Unless Note)*

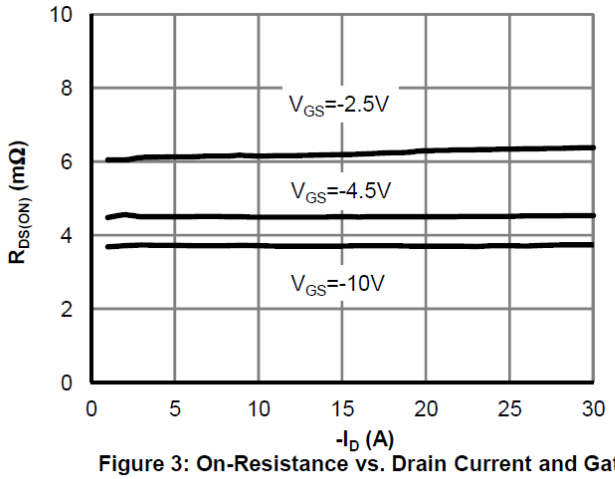


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

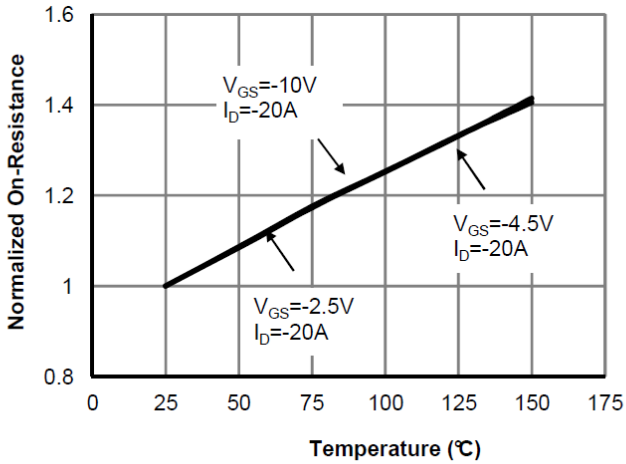


Figure 4: On-Resistance vs. Junction Temperature (Note E)

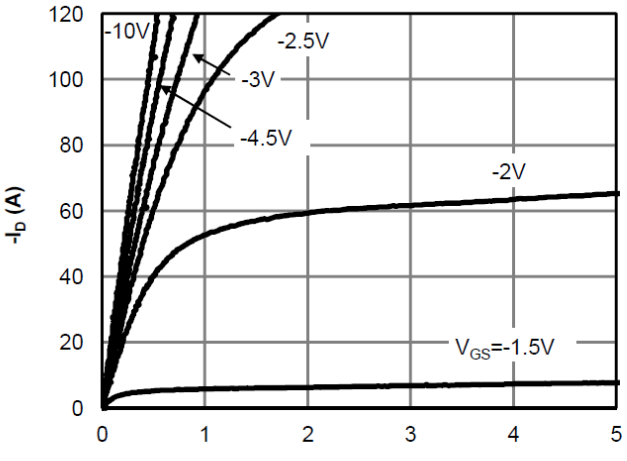


Fig 1: On-Region Characteristics (Note E)

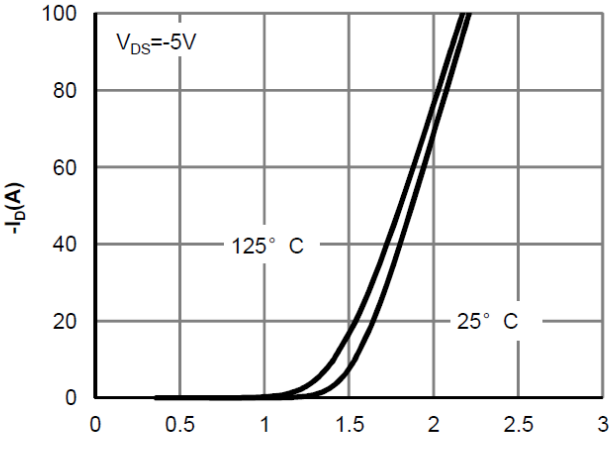


Figure 2: Transfer Characteristics (Note E)

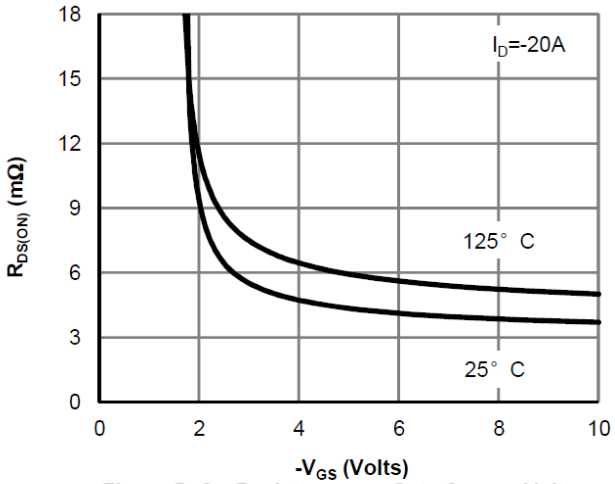


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

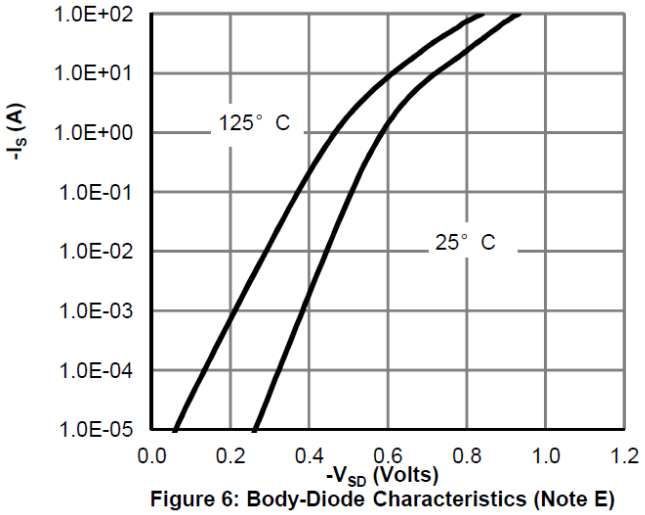
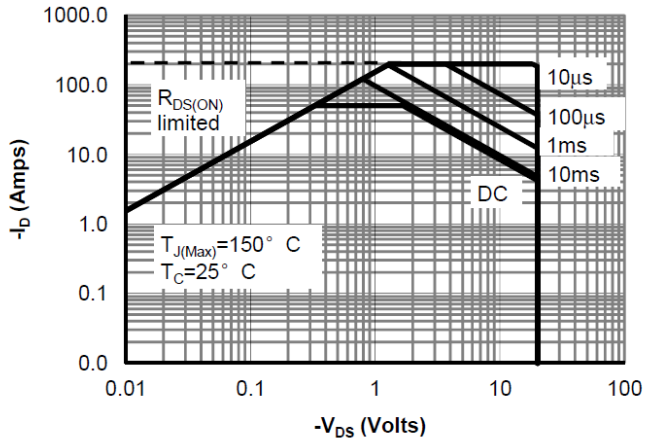


Figure 6: Body-Diode Characteristics (Note E)

■ *TYPICAL CHARACTERISTICS (continuous)*



VGS> or equal to 2.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

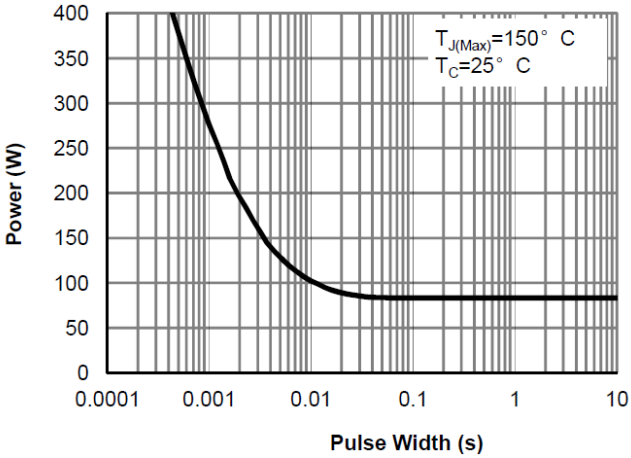


Figure 10: Single Pulse Power Rating Junction-to-Ca (Note F)

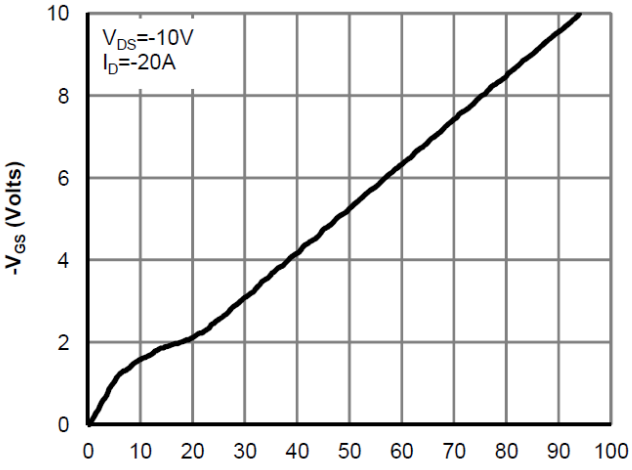


Figure 7: Gate-Charge Characteristics

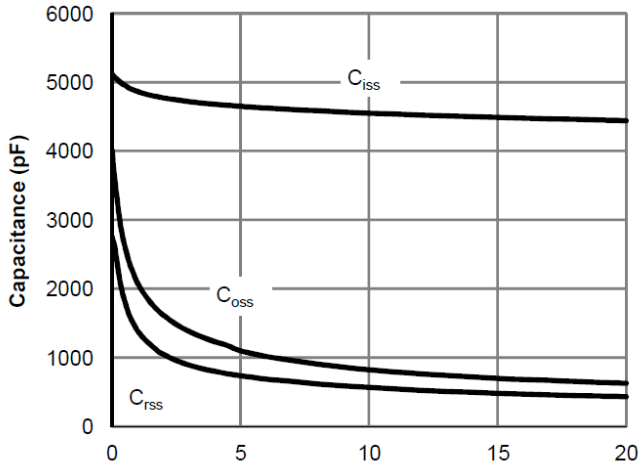


Figure 8: Capacitance Characteristics

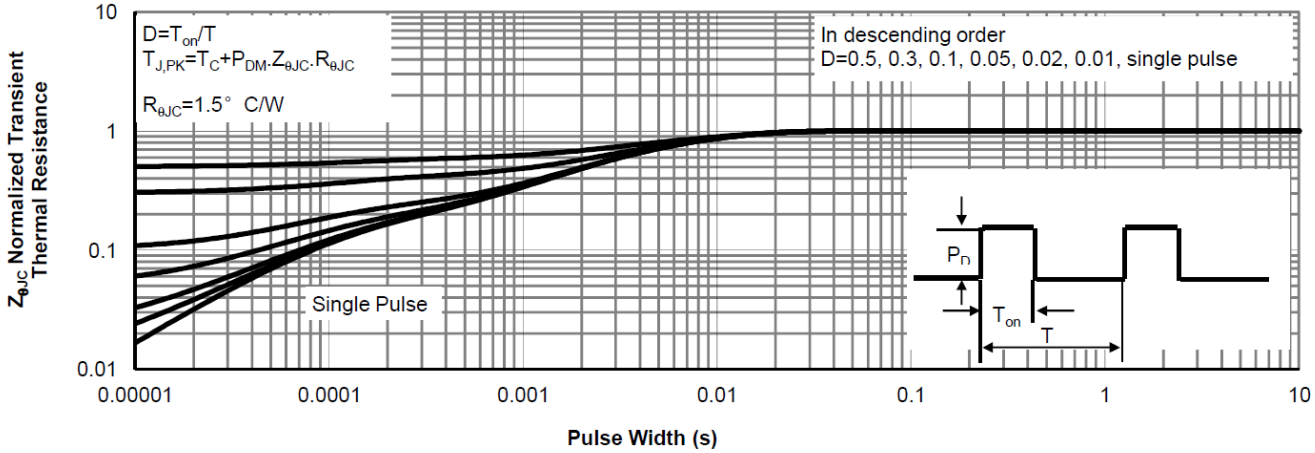
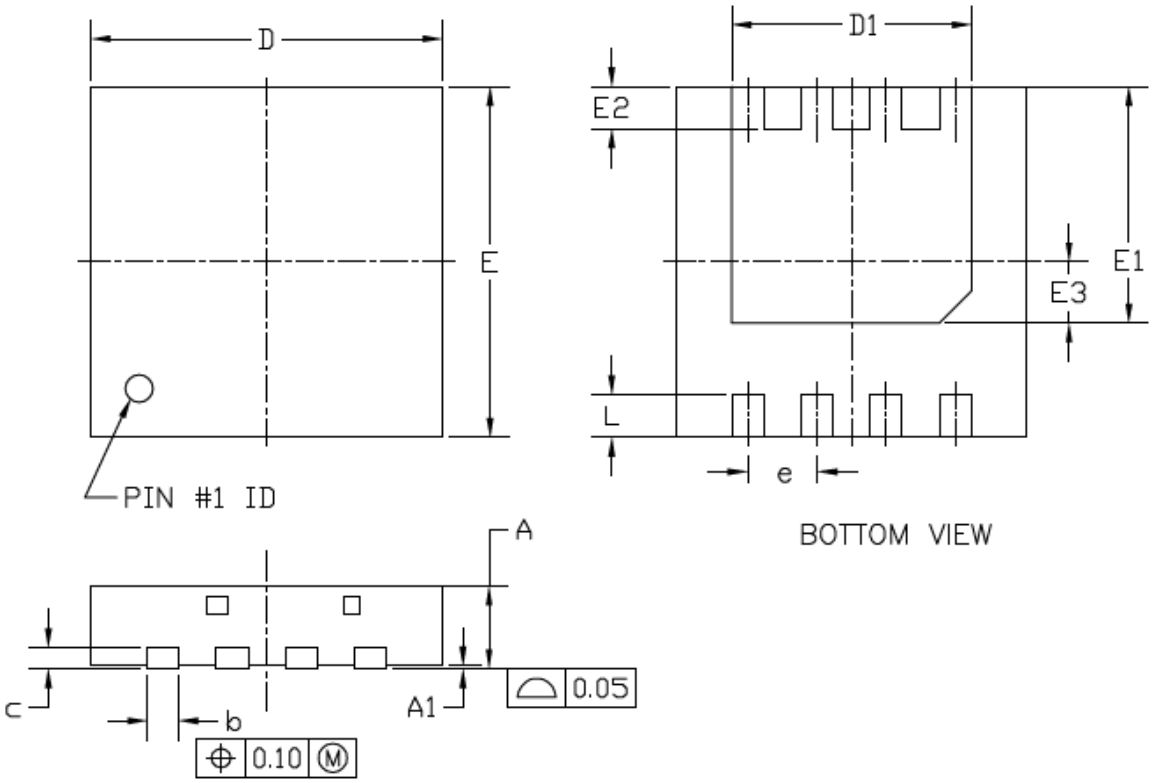
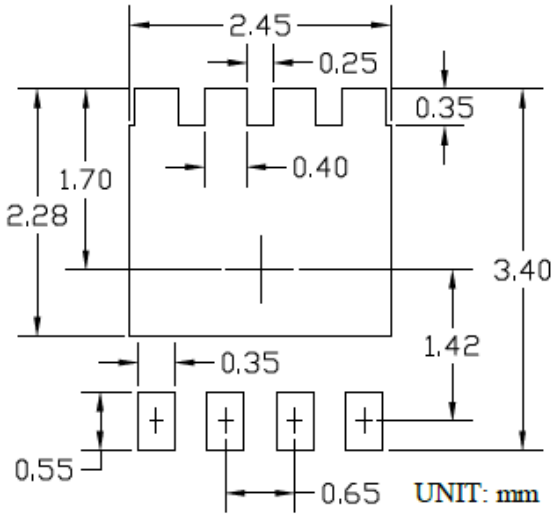


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

■ *DFN3.3X3.3 EP-8L PACKAGE OUTLINE DIMENSIONS*



RECOMMENDED LAND PATTERN

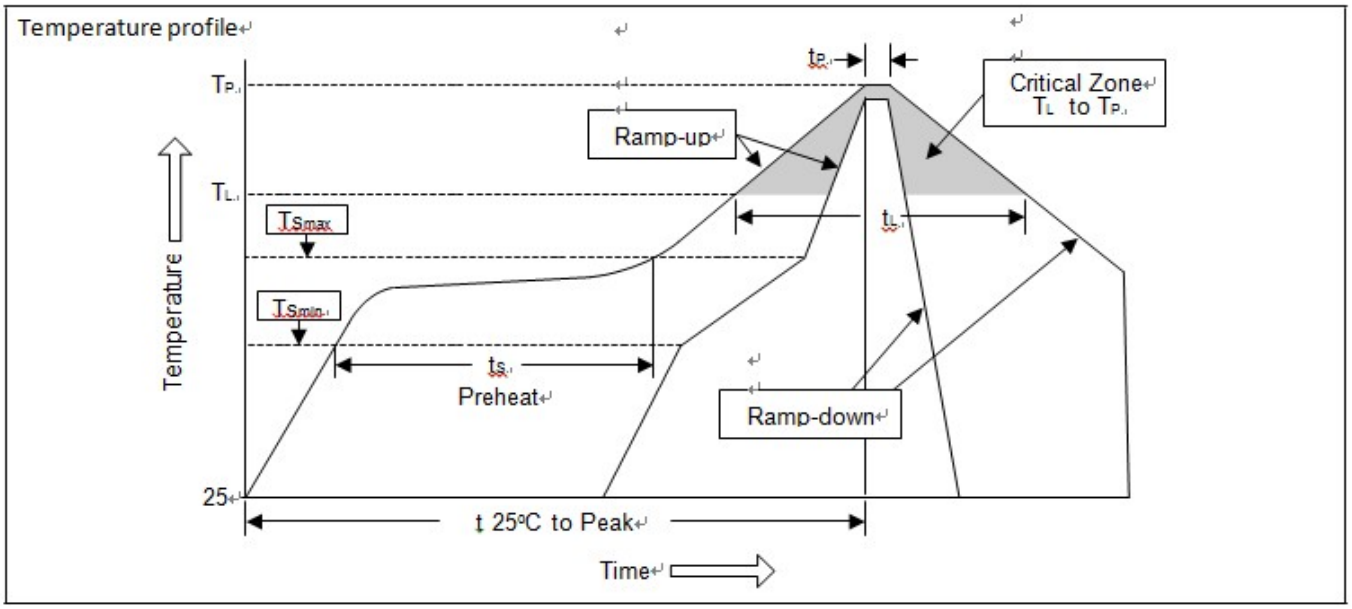


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	--	--	0.05	--	--	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.15	0.25	0.004	0.006	0.010
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.15	2.25	2.35	0.085	0.089	0.093
E2	0.30	0.40	0.50	0.012	0.016	0.020
E3	0.48	0.58	0.68	0.019	0.023	0.027
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

■ *SOLDERING METHODS FOR UNIVERCHIP*

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3℃/sec	<3℃/sec
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	 100℃ 150℃ 60~120 sec	 150℃ 200℃ 60~180 sec
Tsmax to T_L -Ramp-up Rate	<3℃/sec	<3℃/sec
Time maintained above -Temperature (T_L) -Time (t_L)	 183℃ 60~150 sec	 217℃ 60~150 sec
Peak Temperature (T_P)	240℃+0/-5℃	260℃+0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6℃/sec	<6℃/sec
Time 25℃ to Peak Temperature	<6 minutes	<6 minutes

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time

Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.