# 20V Dual N-Channel Enhancement Mode MOSFET

## DESCRIPTION

The UT5820 is the Dual N-Channel logic enhancement mode power field effect transistor which is produced using high cell density advanced trench technology to provide excellent $R_{DS(ON)}$.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-lin power loss are needed in a very small outline surface mount package

## FEATURE

- ***20V/10A, $R_{DS(ON)}$=7mΩ (typ.)@VGS=4.5V***
- ***20V/10A, $R_{DS(ON)}$=9mΩ (typ.)@VGS=2.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- This is a Full RoHS compliance
- DFN2 x 5 package design
- ESD Rating:2000V HBM

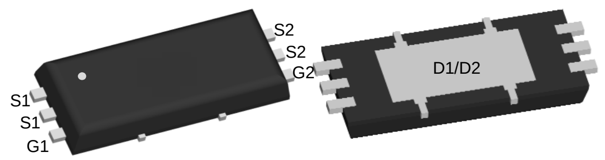
## APPLICATIONS

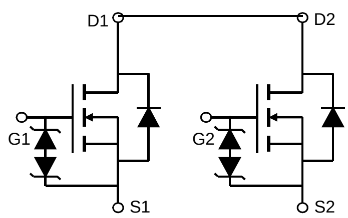
- Power Management in Note Book
- Portable Equipment
- Battery Powered System

## PIN CONFIGURATION

**DFN 2X5**

**Top View** **Bottom View**




## PART NUMBER INFORMATION

| | |
|---|---|
| UT5820AA-BB C | A=Package Code<br>T: DFN2x5<br>BB=Handing Code<br>TR: Tape&Reel<br>C=Lead Plating Code<br>G: Green Product |

## ORDERING INFROMATION

| Part Number | Package Code | Package | Shipping |
|---|---|---|---|
| UT5820 AT-TRG | T | TSSOP8 | 3000EA / T&R |

※ Year Code : 0~9

※ Week Code : A~Z(1-26); a~z(27~52)

※ G : Green Product. This product is RoHS compliant.

## ABSOLUTE MAXIMUM RATINGS *( $T_A$ = 25℃ Unless otherwise noted )*

| Parameter | | Symbol | Maximum | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±12 | V |
| Continuous Drain Current [A] | $T_A$=25°C | $I_D$ | 10 | A |
| | $T_A$=70°C | | 8 | |
| Pulsed Drain Current [B] | | $I_{DM}$ | 85 | |
| Power Dissipation [A] | $T_A$=25°C | $P_D$ | 1.7 | W |
| | $T_A$=70°C | | 1 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | °C |

**Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied**

## THERMAL DATA

| Thermal Characteristics | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Typ** | **Max** | **Units** |
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 64 | 83 | °C/W |
| Maximum Junction-to-Ambient [A] | Steady-State | | 89 | 120 | °C/W |
| Maximum Junction-to-Lead [C] | Steady-State | $R_{\theta JL}$ | 53 | 70 | °C/W |

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

## ■ *ELECTRICAL CHARACTERISTICS(VDD=2.75V, $T_A$=25℃ Unless otherwise noted)*

| Symbol | Parameter | Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250μA, $V_{GS}$=0V | | 20 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=20V, $V_{GS}$=0V | | | | 1 | μA |
| | | | $T_J$=55°C | | | 5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$=±8.0V | | | | ±1 | μA |
| | | $V_{DS}$=0V, $V_{GS}$=±10V | | | | ±10 | μA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=250μA | | 0.3 | 0.6 | 1 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=4.5V, $V_{DS}$=5V | | 30 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=4.5V, $I_D$=7A | | 5 | 7 | 9 | mΩ |
| | | | $T_J$=125°C | 8 | 11 | 13 | |
| | | $V_{GS}$=4.0V, $I_D$=7A | | 5.5 | 7.5 | 10 | mΩ |
| | | $V_{GS}$=3.1V, $I_D$=6.5A | | 6.3 | 8.3 | 11 | mΩ |
| | | $V_{GS}$=2.5V, $I_D$=5.5A | | 6.8 | 9.0 | 13 | mΩ |
| | | $V_{GS}$=1.8V, $I_D$=5A | | | 13 | 18 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=7A | | | 65 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | | 0.7 | 1.3 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | | 2.5 | A |
| **DYNAMIC PARAMETERS** | | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=10V, f=1MHz | | | 1120 | | pF |
| $C_{oss}$ | Output Capacitance | | | | 195 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | | 155 | | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | | | 4.0 | | Ω |
| **SWITCHING PARAMETERS** | | | | | | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$=4.5V, $V_{DS}$=10V, $I_D$=10A | | | 16 | | nC |
| $Q_{gs}$ | Gate Source Charge | | | | 1.7 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | | 6.8 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=5V, $V_{DS}$=10V, $R_L$=1.35Ω, $R_{GEN}$=3Ω | | | 18 | | ns |
| $t_r$ | Turn-On Rise Time | | | | 27 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | | 64 | | ns |
| $t_f$ | Turn-Off Fall Time | | | | 42 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=10A, dI/dt=500A/μs | | | 12 | | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=10A, dI/dt=500A/μs | | | 16 | | nC |

**Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%**

**2.Static parameters are based on package level with recommended wire bonding**

## ■ *TYPICAL CHARACTERISTICS (25℃ Unless Note)*

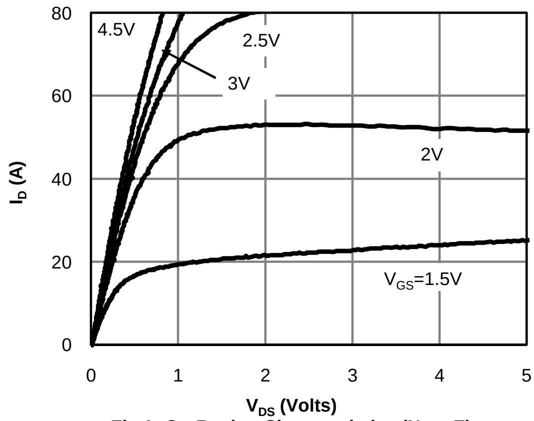



Fig 1: On-Region Characteristics (Note E)

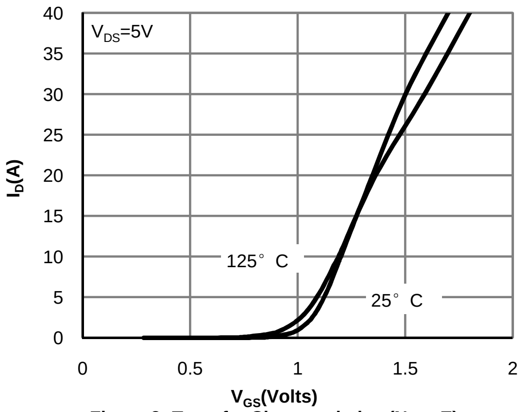



Figure 2: Transfer Characteristics (Note E)

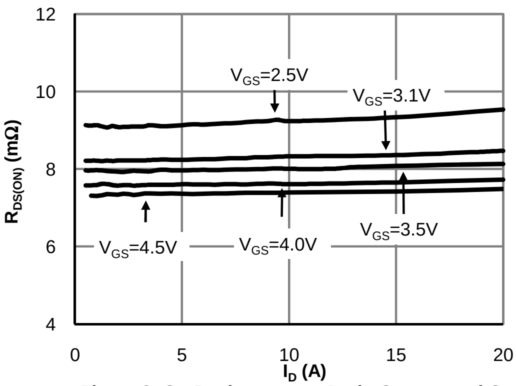



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

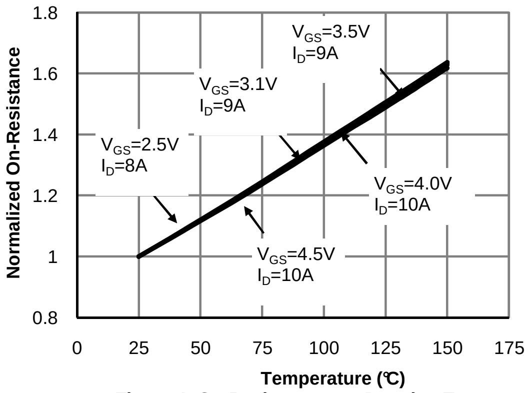



Figure 4: On-Resistance vs. Junction Temperature (Note E)

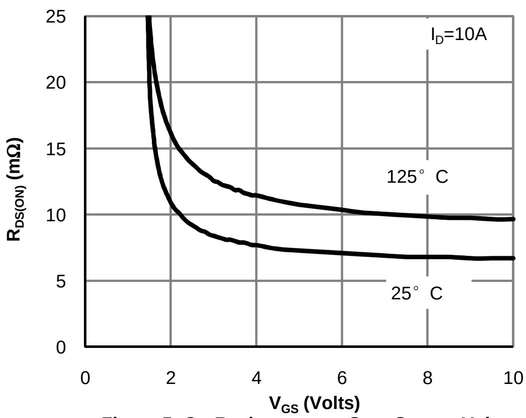



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

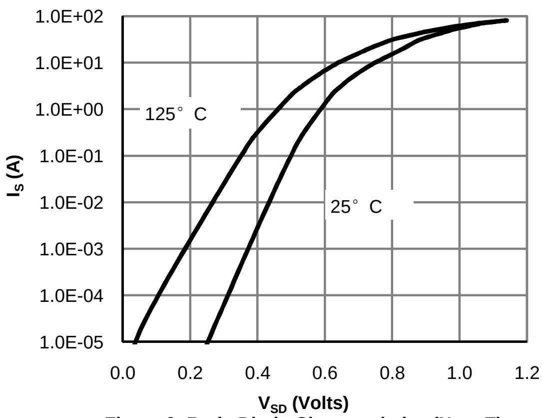



Figure 6: Body-Diode Characteristics (Note E)

## ■ *TYPICAL CHARACTERISTICS* *(continuous)*

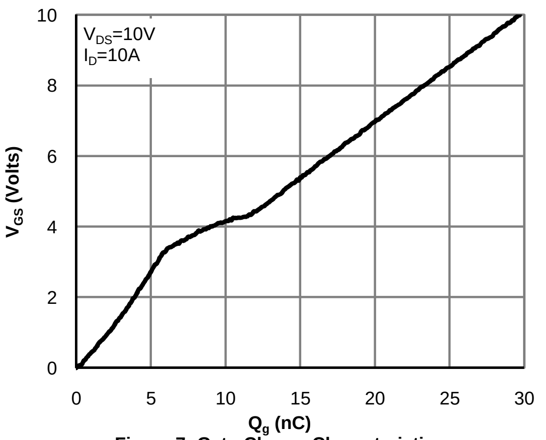



**Figure 7: Gate-Charge Characteristics**

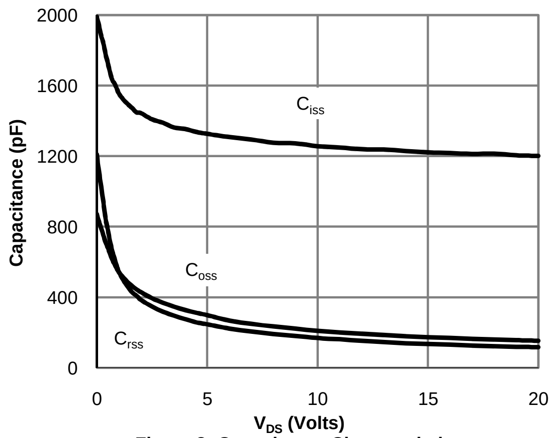



**Figure 8: Capacitance Characteristics**

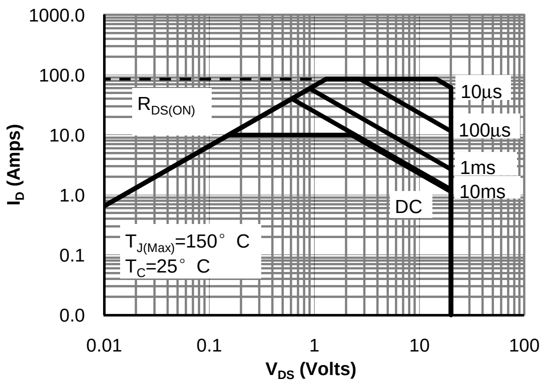



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

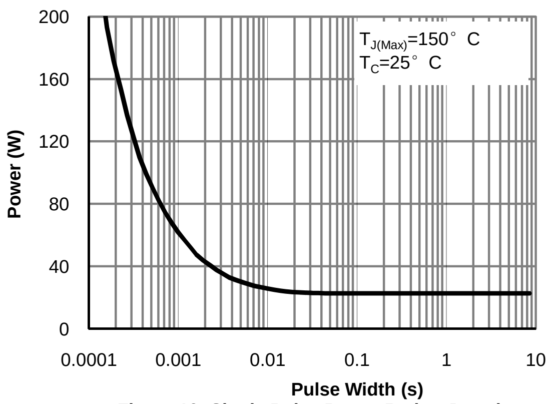



**Figure 10: Single Pulse Power Rating Junction-to-Ca (Note F)**

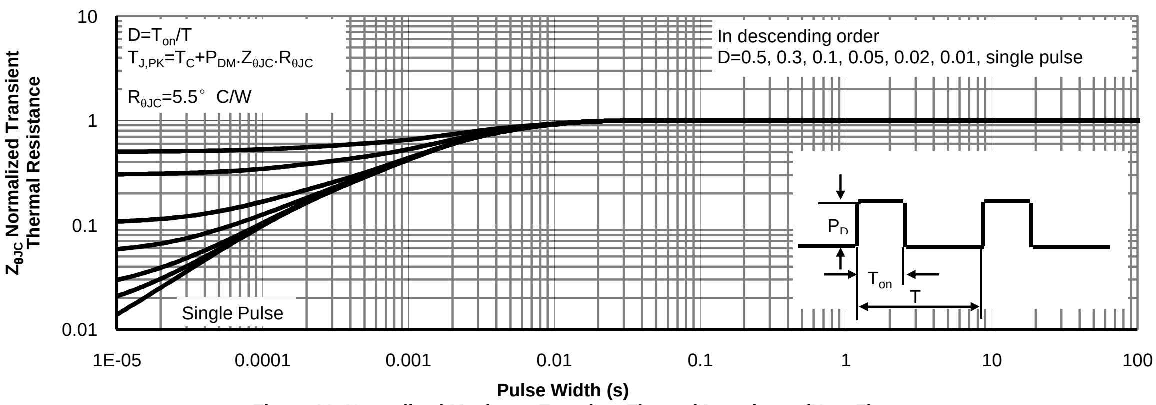
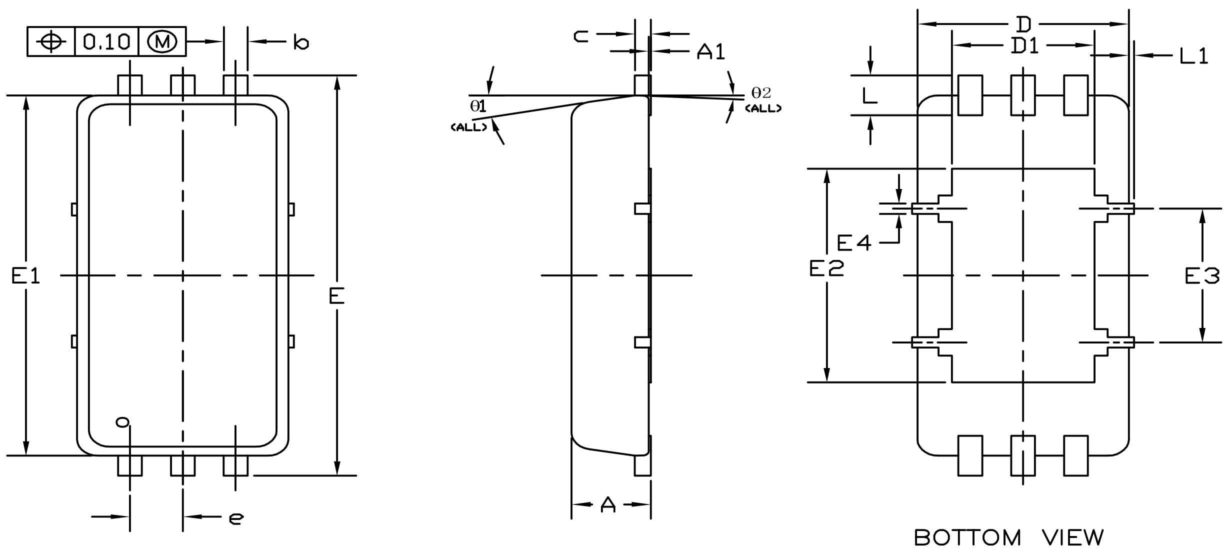


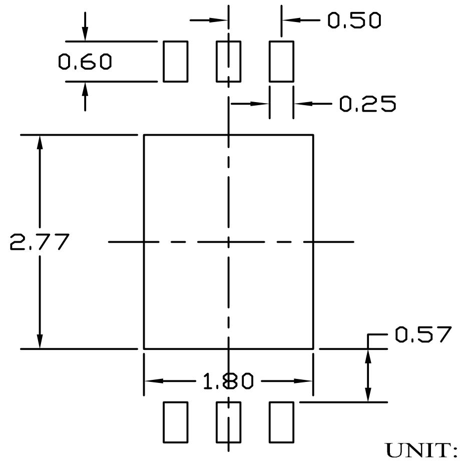

**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

## DFN2X5 PACKAGE OUTLINE DIMENSIONS

DFN2x5_6L_EP1_P PACKAGE OUTLINE




RECOMMENDED LAND PATTERN




UNIT: mm

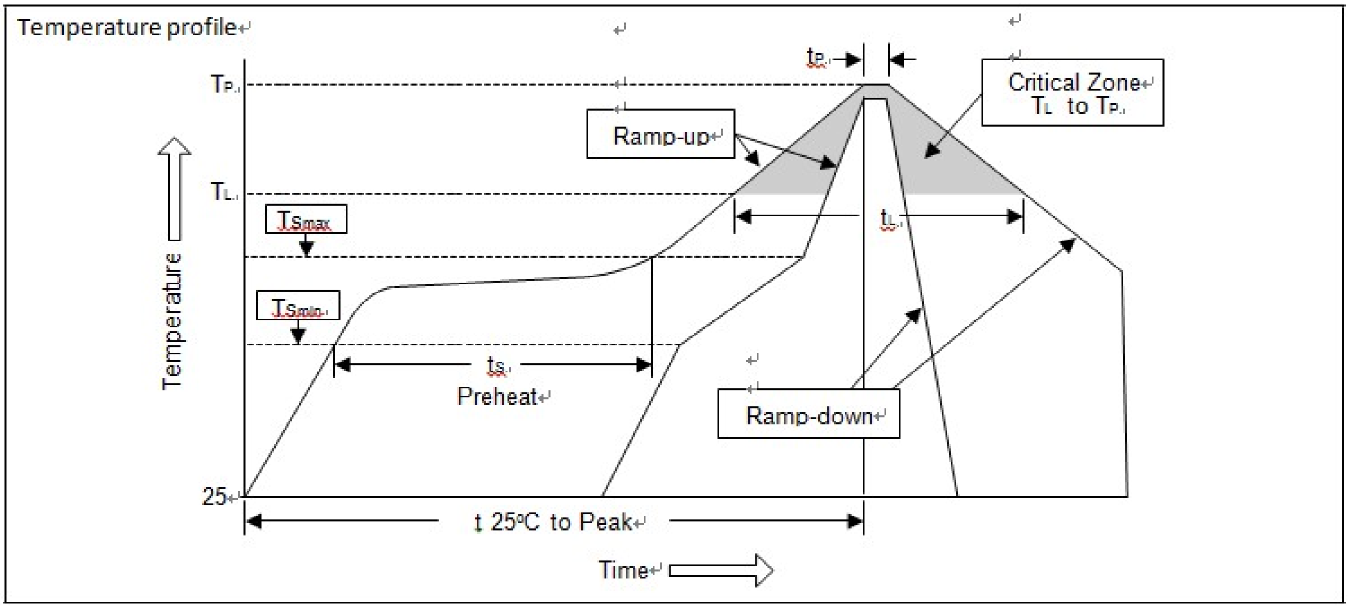
| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | —— | 0.05 | 0.000 | —— | 0.002 |
| b | 0.20 | 0.23 | 0.30 | 0.008 | 0.009 | 0.012 |
| c | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | | 2.00 BSC | | | 0.079 BSC | |
| D1 | 1.30 | 1.35 | 1.55 | 0.051 | 0.053 | 0.061 |
| E | | 5.00 BSC | | | 0.197 BSC | |
| E1 | | 4.50 BSC | | | 0.177 BSC | |
| E2 | 2.60 | 2.67 | 2.95 | 0.102 | 0.105 | 0.116 |
| E3 | | 1.67 BSC | | | 0.066 BSC | |
| E4 | | 0.13 BSC | | | 0.005 BSC | |
| e | | 0.50 BSC | | | 0.020 BSC | |
| L | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |
| L1 | 0 | --- | 0.10 | 0 | --- | 0.004 |
| θ1 | 0° | 10° | 12° | 0° | 10° | 12° |
| θ2 | | 3° BSC | | | 3° BSC | |

NOTE
1. PAKCAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MIL EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

## SOLDERING METHODS FOR UNIVERCHIP

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device




| Profile Feature | Sn-Pb Eutectic Assembly | Pb free Assembly |
|---|---|---|
| Average ramp-up rate ($T_L$ to $T_P$) | <3℃/sec | <3℃/sec |
| Preheat<br>-Temperature Min ($Ts_{min}$)<br>-Temperature Max ($Ts_{max}$)<br>-Time (min to max) (ts) | <br>100℃<br>150℃<br>60~120 sec | <br>150℃<br>200℃<br>60~180 sec |
| Tsmax to $T_L$<br>-Ramp-up Rate | <3℃/sec | <3℃/sec |
| Time maintained above<br>-Temperature ($T_L$)<br>-Time ($t_L$) | <br>183℃<br>60~150 sec | <br>217℃<br>60~150 sec |
| Peak Temperature ($T_P$) | 240℃+0/-5℃ | 260℃+0/-5℃ |
| Time within 5℃ of actual Peak Temperature ($t_P$) | 10~30 sec | 20~40 sec |
| Ramp-down Rate | <6℃/sec | <6℃/sec |
| Time 25℃ to Peak Temperature | <6 minutes | <6 minutes |

Flow (wave) soldering (solder dipping)

| Product | Peak Temperature | Dipping Time |
|---|---|---|
| Pb device | 245℃±5℃ | 5sec±1sec |
| Pb-Free device | 260℃+0/-5℃ | 5sec±1sec |

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.