Desemicore

D516

30V N-Channel Enhancement Mode MOSFET

■ *DESCRIPTION*

The UC516 is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance.

This device is suitable for use as a load switch or in PWM and gate charge for most of the synchronous buck converter applications

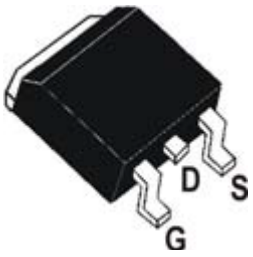
■ *FEATURE*

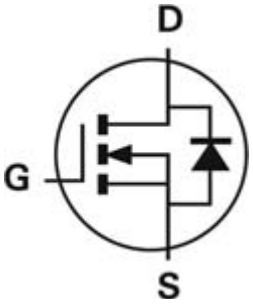
- ***I_D=72A***
- ***$R_{DS(ON)}$<6.0mΩ @V_{GS}=10V***
- ***$R_{DS(ON)}$<8.5mΩ @V_{GS}=4.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- TO-252 package design

■ *APPLICATIONS*

- Motor / Body Load Control
- Automotive Systems
- Solenoid and Motor Control
- DC-DC converters

■ *PIN CONFIGURATION*





■ PART NUMBER INFORMATION

UC516A-BB C	A= Package Code T: TO-252 BB=Handing Code TR: Tape&Reel C=Lead Plating Code G: Green Product

■ ORDERING INFROMATION

Part Number	Package Code	Package	Shipping
UC516T-TRG	T	TO252	2500EA / T&R

※ Year Code : 0~9

※ Week Code : A~Z(1-26); a~z(27~52)

※ G : Green Product. This product is RoHS compliant.

■ ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current (T_A=25℃)	V_{GS}=10V	72	A
	Continuous Drain Current (T_A=70℃)		57	A
I_{DM}	Pulsed Drain Current		210	A
I_{AS}	Avalanche Current		30	A
E_{AS}	Avalanche Energy, L=0.1mH		45	mJ
P_D	Power Dissipation	T_A=25℃	50	W
		T_A=70℃	32	
T_J	Operation Junction Temperature		-55~+150	℃
T_{STG}	Storage Temperature Range		-55~+150	℃
$R_{\Theta JA}$	Thermal Resistance Junction to Ambient		50	℃/W
$R_{\Theta JC}$	Thermal Resistance Junction to Case		2.5	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

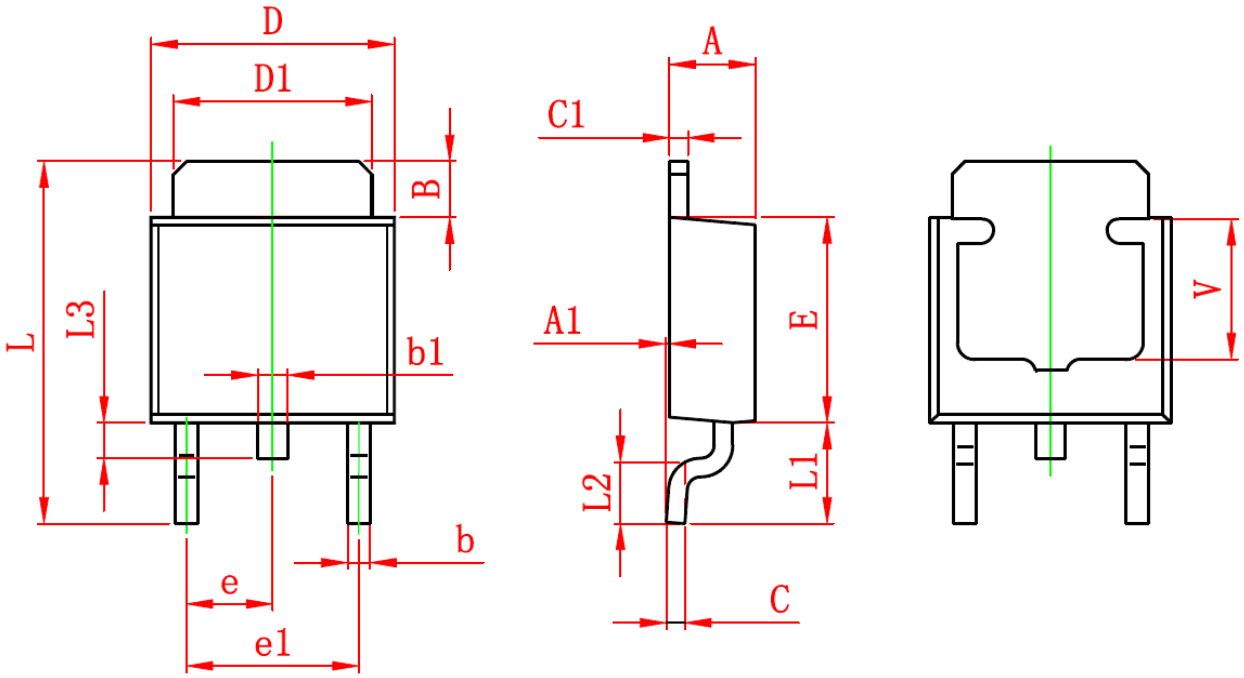
■ *ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BV)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.2		2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0			1	uA
		V_{DS}=24V, V_{GS}=0 T_J=55℃			5	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=19A		4.5	6	mΩ
		V_{GS}=4.5V, I_D=16A		6.5	8.0	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=10A, V_{GS}=0V			1.3	V
t_{rr}	Body Diode Reverse Recovery Time	I_F=10A, dI/dt=100A/us		26		nS
Q_{rr}	Body Diode Reverse Recovery Charge			18		nC
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=15V V_{GS}=4.5V I_D=10A		12		nC
Q_{gs}	Gate-Source Charge			6		
Q_{gd}	Gate-Drain Charge			5		
C_{iss}	Input Capacitance	V_{DS}=15V V_{GS}=0V f=1MHz		1750		pF
C_{oss}	Output Capacitance			360		
C_{rss}	Reverse Transfer Capacitance			150		
$T_{d(on)}$	Turn-On Time	V_{DS}=15V I_D=10A V_{GS}=4.5V R_{GEN}=3Ω		24		nS
T_r				21		
$T_{d(off)}$	Turn-Off Time			25		
T_f				17		

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

2.Static parameters are based on package level with recommended wire bonding

■ *TO-252 PACKAGE OUTLINE DIMENSIONS*

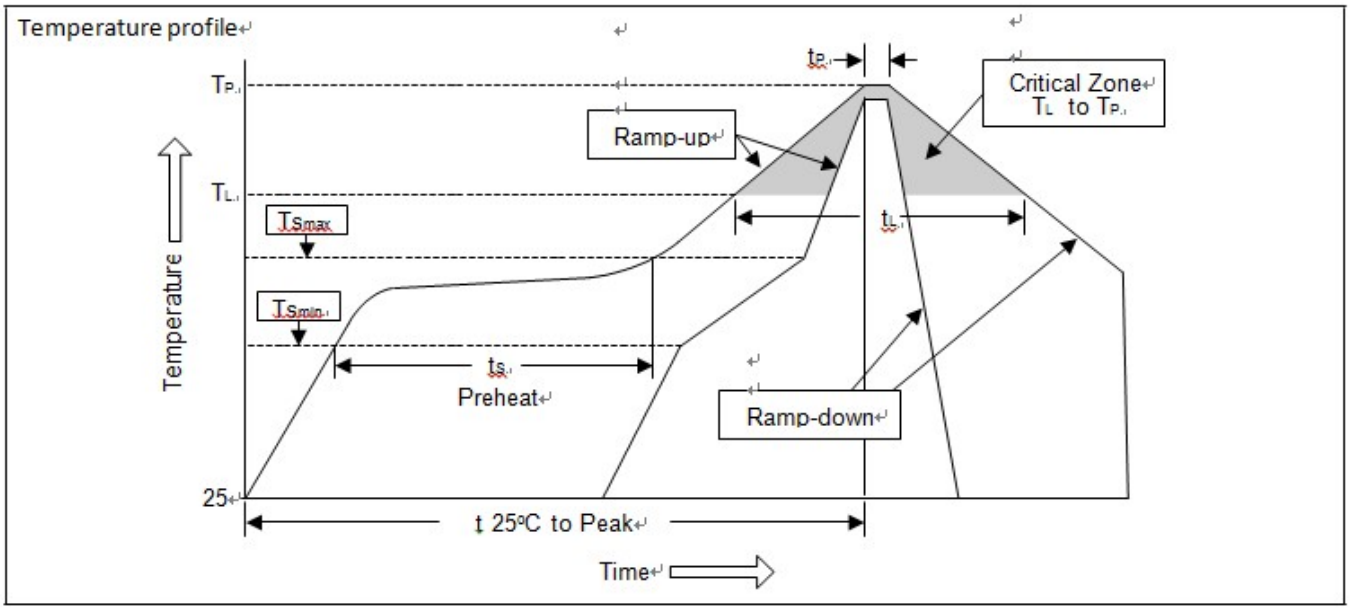


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP		0.091 TYP	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
V	3.80 REF		0.150 REF	

■ *SOLDERING METHODS FOR UNIVERCHIP*

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3℃/sec	<3℃/sec
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	 100℃ 150℃ 60~120 sec	 150℃ 200℃ 60~180 sec
Tsmax to T_L -Ramp-up Rate	<3℃/sec	<3℃/sec
Time maintained above -Temperature (T_L) -Time (t_L)	 183℃ 60~150 sec	 217℃ 60~150 sec
Peak Temperature (T_P)	240℃+0/-5℃	260℃+0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6℃/sec	<6℃/sec
Time 25℃ to Peak Temperature	<6 minutes	<6 minutes

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.