60V Complementary Enhancement Mode MOSFET

■ *DESCRIPTION*

The 4612 is the complementary enhancement mode power field effect transistor is produced using high cell density advanced trench technology to provide excellent $R_{DS(ON)}$.

This device is suitable for use as a load switch or in PWM and gate charge for most of the synchronous buck converter applications

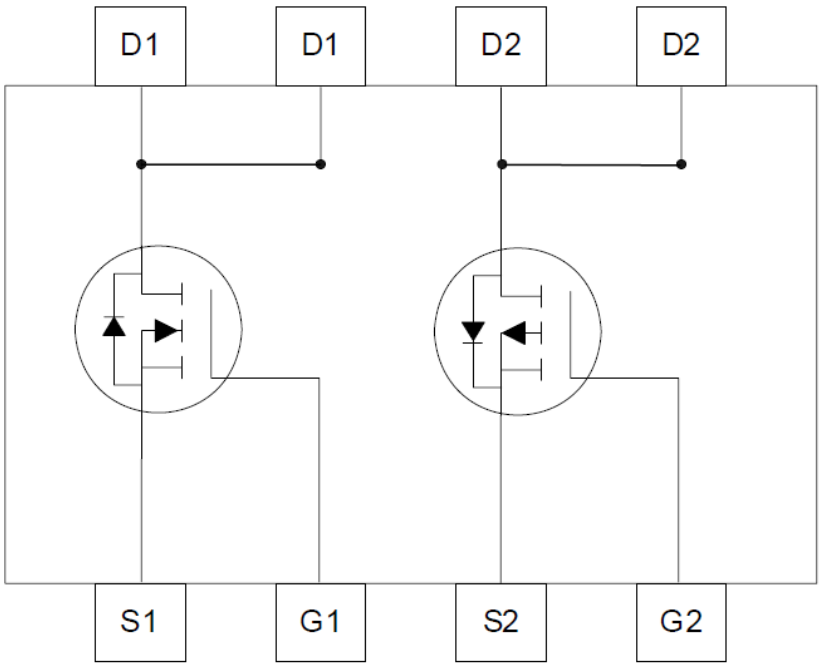
■ *FEATURE*

- ***60V/4.5A, $R_{DS(ON)}$=37mΩ @V_{GS}=10V N_CH***
- ***-60V/-3.5A, $R_{DS(ON)}$=70mΩ @V_{GS}=-10V P_CH***
- ***60V/4.0A, $R_{DS(ON)}$=42mΩ @V_{GS}=4.5V N_CH***
- ***-60V/-3.0A, $R_{DS(ON)}$=93mΩ @V_{GS}=-4.5V P_CH***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- SOP8 package design

■ *APPLICATIONS*

- High Frequency Point-of-Load Synchronous
- New working DC-DC Power System
- Load Switch

■ *PIN CONFIGURATION*



■ PART NUMBER INFORMATION

4612A-BB C	A= Package Code S: SOP BB=Handing Code TR: Tape&Reel C=Lead Plating Code G: Green Product

■ ORDERING INFROMATION

Part Number	Package Code	Package	Shipping
4612S-TR	S	SOP8	2500EA / T&R

※ Year Code : 0~9

※ Week Code : A~Z

※ G : Green Product. This product is RoHS compliant.

■ ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter			N-Channel	P-Channel	Unit
V_{DSS}	Drain-Source Voltage			60	-60	V
V_{GSS}	Gate-Source Voltage			±20	±20	V
I_D	Continuous Drain Current (T_A=25℃)		V_{GS}=10V	4.5	-3.5	A
	Continuous Drain Current (T_A=70℃)			3.6	-2.8	A
I_{DM}	Pulsed Drain Current			20	-20	A
P_D	Power Dissipation	T_A=25℃		1	1	W
		T_A=70℃		0.8	0.8	
T_J	Operation Junction Temperature			-55~150	-55~150	℃
T_{STG}	Storage Temperature Range			-55~150	-55~150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ *N Channel ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.0	1.7	2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=48V, V_{GS}=0			1	uA
		V_{DS}=48V, V_{GS}=0 T_J=55℃			30	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=4.5A		37	58	mΩ
		V_{GS}=4.5V, I_D=4.0A		42	60	
g_{FS}	Forward Transconductance	V_{DS}=10V, I_D=4.5A		6		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V		0.76	1.0	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=30V		14	16	nC
Q_{gs}	Gate-Source Charge	V_{GS}=10V		3.9		
Q_{gd}	Gate-Drain Charge	I_D=4.5A		4.7		
C_{iss}	Input Capacitance	V_{DS}=15V		418	588	pF
C_{oss}	Output Capacitance	V_{GS}=0V		65		
C_{rss}	Reverse Transfer Capacitance	f=1MHz		52		
$T_{d(on)}$	Turn-On Time	V_{DS}=30V		8	20	nS
T_r		V_{GS}=10V		12	18	
$T_{d(off)}$	Turn-Off Time	R_G=6Ω		30	35	
T_f		R_L=15Ω		7	15	

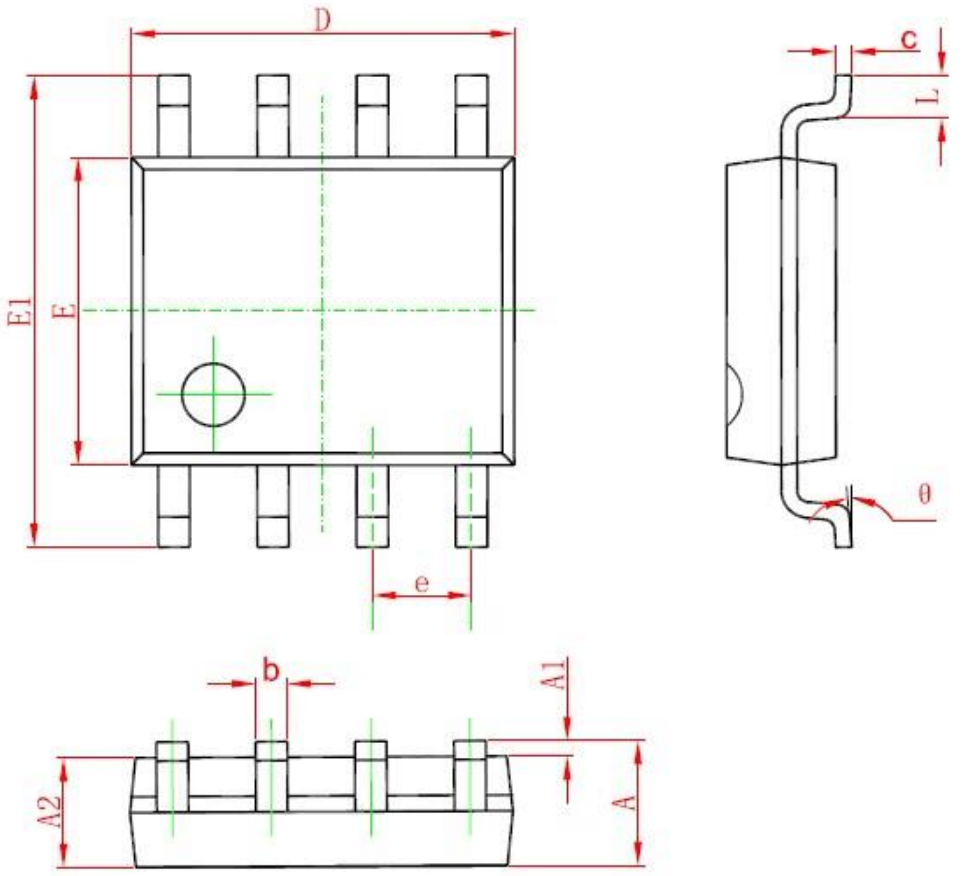
Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

2.Static parameters are based on package level with recommended wire bonding

■ *P Channel ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.0	-1.8	-2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-48V, V_{GS}=0			-1	uA
		V_{DS}=-48V, V_{GS}=0 T_J=55℃			-30	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D=-3.5A		70	90	mΩ
		V_{GS}=-4.5V, I_D=-3A		93	125	
g_{FS}	Forward Transconductance	V_{DS}=-10V, I_D=-3.5A		5		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=-1.0A, V_{GS}=0V		-0.77	-1.0	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=-30V		10	15	nC
Q_{gs}	Gate-Source Charge	V_{GS}=-10V		3		
Q_{gd}	Gate-Drain Charge	I_D=-3.5A		3.1		
C_{iss}	Input Capacitance	V_{DS}=-30V		940		pF
C_{oss}	Output Capacitance	V_{GS}=0V		49		
C_{rss}	Reverse Transfer Capacitance	f=1MHz		35		
$T_{d(on)}$	Turn-On Time	V_{DS}=-30V		6	13	nS
T_r		V_{GS}=-10V		8	18	
$T_{d(off)}$	Turn-Off Time	R_G=6Ω		26	31	
T_f		R_L=15Ω		11	20	

■ *SOP8 PACKAGE OUTLINE DIMENSIONS*

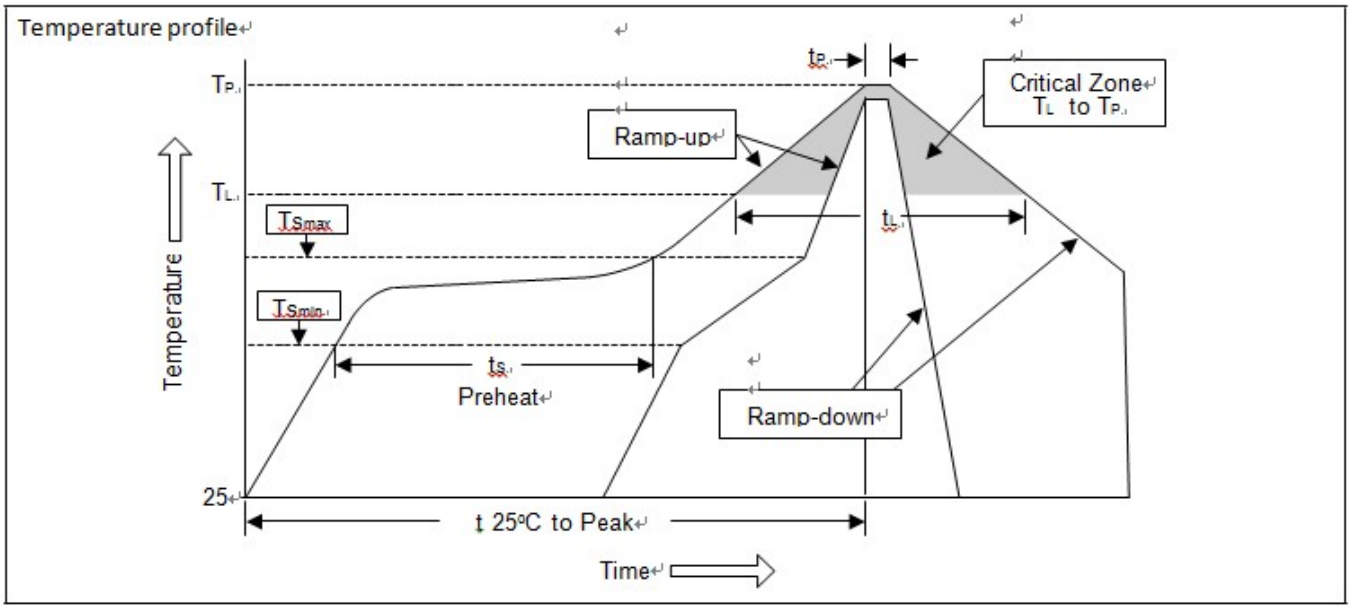


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

■ *SOLDERING METHODS FOR UNIVERCHIP*

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3℃/sec	<3℃/sec
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	 100℃ 150℃ 60~120 sec	 150℃ 200℃ 60~180 sec
Tsmax to T_L -Ramp-up Rate	<3℃/sec	<3℃/sec
Time maintained above -Temperature (T_L) -Time (t_L)	 183℃ 60~150 sec	 217℃ 60~150 sec
Peak Temperature (T_P)	240℃+0/-5℃	260℃+0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6℃/sec	<6℃/sec
Time 25℃ to Peak Temperature	<6 minutes	<6 minutes

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.