Desemicore

D2305A

P-Channel 20V (D-S) MOSFET

GENERAL DESCRIPTION

The ME2305A is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 67m\Omega @ V_{GS}$=-10V
- $R_{DS(ON)} \leqq 77m\Omega @ V_{GS}$=-4.5V
- $R_{DS(ON)} \leqq 96m\Omega @ V_{GS}$=-2.5V
- $R_{DS(ON)} \leqq 125m\Omega @ V_{GS}$=-1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

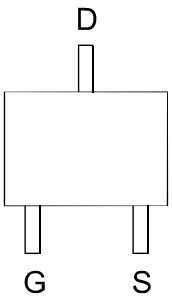
APPLICATIONS

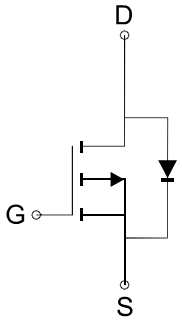
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

(SOT-23)

Top View





P-Channel MOSFET

Ordering Information: ME2305A (Pb-free)

ME2305A-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Steady State	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±8	V
Continuous Drain Current	T_A=25℃	I_D	3.5	A
	T_A=70℃		2.8	
Pulsed Drain Current		I_{DM}	14	A
Maximum Power Dissipation	T_A=25℃	P_D	1.3	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	100	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.4		-1.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±8V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-20V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=-10V, I_D= -4.2A		57	67	mΩ
		V_{GS}=-4.5V, I_D= -3.4A		65	77	
		V_{GS}=-2.5V, I_D= -2.5A		75	96	
		V_{GS}=-1.8V, I_D= -1.7A		95	125	
V_{SD}	Diode Forward Voltage	I_S=-1.2A, V_{GS}=0V		0.8		V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-15V, V_{GS}=-10V, I_D=-4.2A		20		nC
Qg	Total Gate Charge	V_{DS}=-15V, V_{GS}=-4.5V, I_D=-4.2A		10		
Qgs	Gate-Source Charge			2.8		
Qgd	Gate-Drain Charge			2.5		
Ciss	Input capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz		745		pF
Coss	Output Capacitance			65		
Crss	Reverse Transfer Capacitance			21		
td(on)	Turn-On Delay Time	V_{DD}=-15V, R_L=15Ω V_{GEN}=-10V,R_G=6Ω		32		ns
tr	Turn-On Rise Time			18		
td(off)	Turn-Off Delay Time			57		
tf	Turn-Off Fall Time			4.5		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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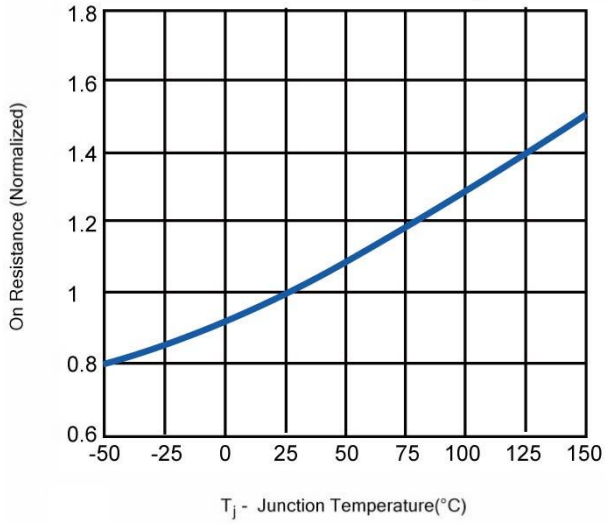
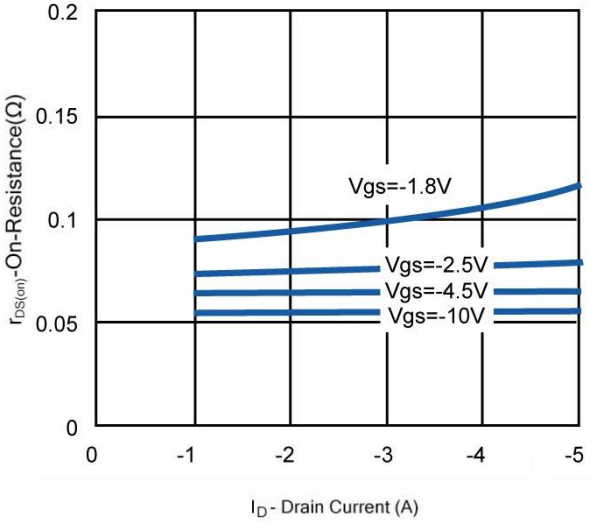
Typical Characteristics (T_J =25℃ Noted)

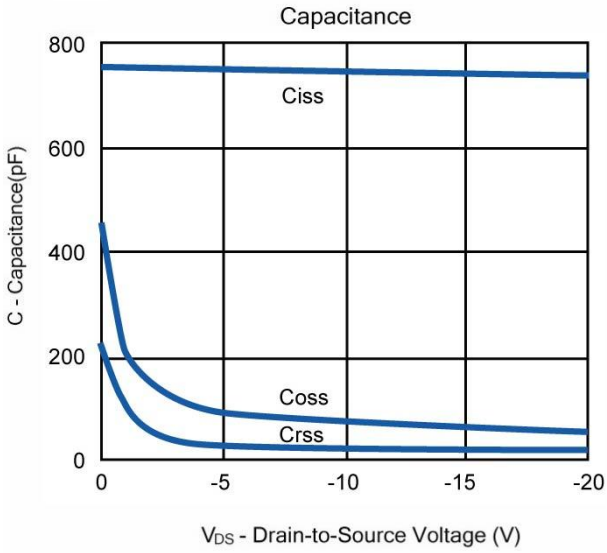
On Resistance vs. Junction Temperature



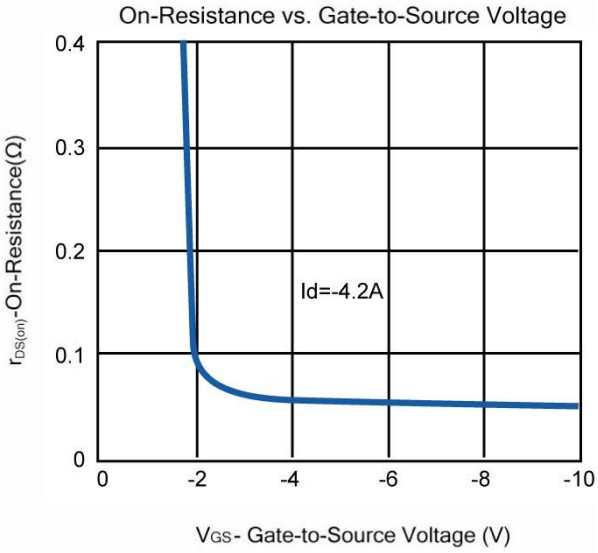
On-Resistance vs. Drain Current



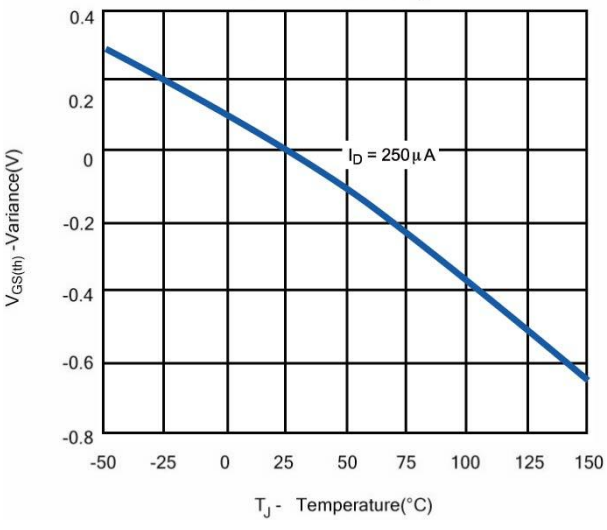
Capacitance



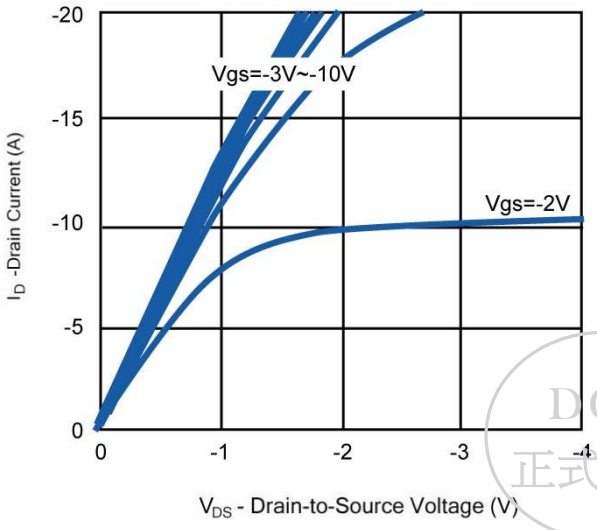
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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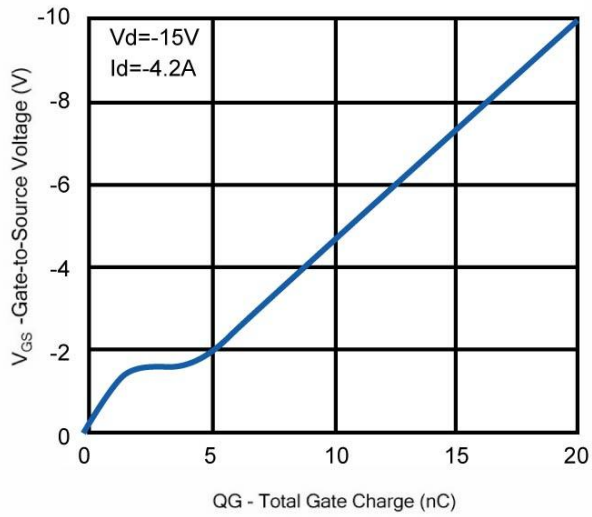
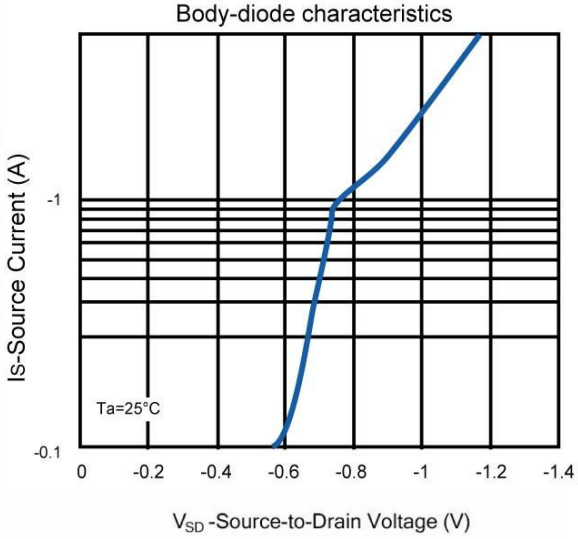
Typical Characteristics (T_J =25℃ Noted)

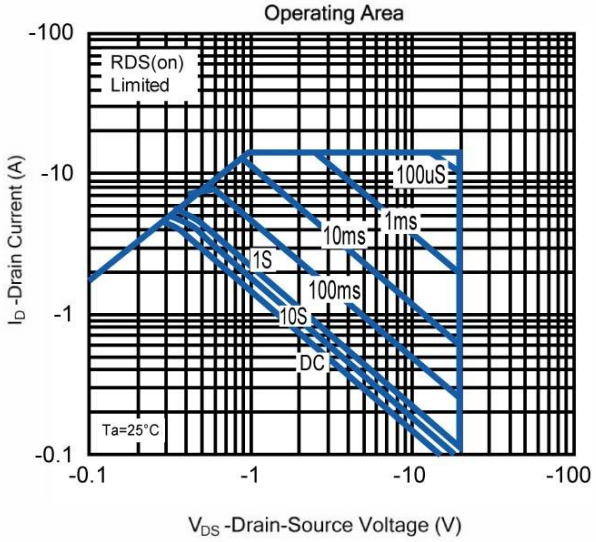
Gate Charge



Body-diode characteristics



Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient