Desemicore

D15N10

100V N-Channel Enhancement Mode MOSFET

■ *DESCRIPTION*

The 15N10 is N channel enhancement mode power effect transitor which is produced using high cell density advanced trench technology.

The high density process is especially able to minize on-state resistance.These devices are. especially suited for low voltage application power management DC-DC converters.

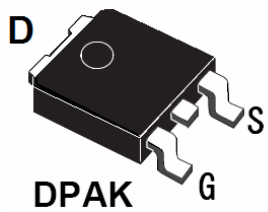
■ *FEATURE*

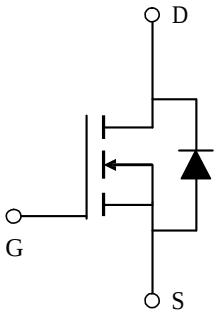
- ***100V/15 A, $R_{DS(ON)}$=80.0mΩ (typ.)@VGS=10V***
- ***100V/8A, $R_{DS(ON)}$=115mΩ(typ.)@VGS= 4.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- TO252 package design
- 100% UIS Tested
- 100% Rg tested

■ *APPLICATIONS*

- Power Management
- DC/DC Converter
- Load Switch

■ *PIN CONFIGURATION*





■ PART NUMBER INFORMATION

15N10AABB C	A= Package Code T: TO-252 BB=Handing Code TR: Tape&Reel C=Lead Plating Code G: Green Product P: Pb free

■ ORDERING INFORMATION

Part Number	Package Code	Package	Shipping
15N10AT-TRG	T	TO-252	2500EA / T&R

※ Year Code : 0~9
※ Week Code : A~Z(1-26); a~z(27~52)
※ G : Green Product. This product is RoHS compliant.

■ ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter		Rating	Unit
Common Ratings (T_A=25°C Unless Otherwise Noted)				
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		±20	
T_J	Maximum Junction Temperature		175	°C
T_{STG}	Storage Temperature Range		-55 to 175	°C
I_S	Diode Continuous Forward Current		5	A
I_{DP}	300μs Pulse Drain Current Tested	T_C=25°C	64	A
		T_C=100°C	44	
I_D	Continuous Drain Current	T_C=25°C	15	A
		T_C=100°C	11	
P_D	Maximum Power Dissipation	T_C=25°C	60	W
		T_C=100°C	30	
$R_{\theta JC}$	Thermal Resistance-Junction to Case		2.5	°C/W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		50	°C/W
E_{AS}	Avalanche Energy, Single Pulsed (L=0.3mH)		30	mJ

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

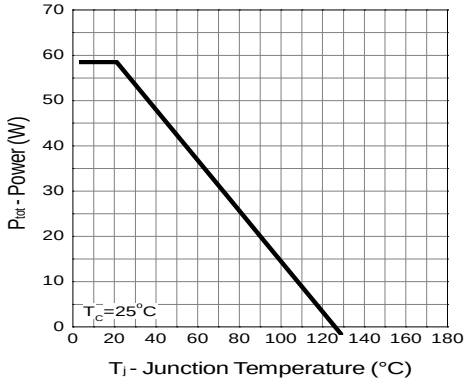
■ *ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

Symbol	Parameter	Test Conditions	UT15N10			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250μA	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V	-	-	1	μA
		T_J=85°C	-	-	30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250μA	1.5	2	2.5	V
I_{GSS}	Gate Leakage Current	V_{GS}=±16V, V_{DS}=0V	-	-	±10	μA
$R_{DS(ON)}$ [a]	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=15A	-	80	100	mΩ
		V_{GS}=4.5V, I_{DS}=8A	-	115	130	
Diode Characteristics						
V_{SD} [a]	Diode Forward Voltage	I_{SD}=5A, V_{GS}=0V	0.6	0.8	1.1	V
t_{rr}	Reverse Recovery Time	I_{DS}=5A, dI_{SD}/dt=100A/μs	33	47	61	ns
Q_{rr}	Reverse Recovery Charge		61	87	113	nC
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, Frequency=1.0MHz	730	940	1250	pF
C_{oss}	Output Capacitance		45	80	115	
C_{rss}	Reverse Transfer Capacitance		25	50	75	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=30V, R_L=30Ω, I_{DS}=1A, V_{GEN}=10V, R_G=6Ω	-	13	24	ns
t_r	Turn-on Rise Time		-	10	19	
$t_{d(OFF)}$	Turn-off Delay Time		-	32	60	
t_f	Turn-off Fall Time		-	16	30	
Gate Charge Characteristics [b]						
Q_g	Total Gate Charge	V_{DS}=50V, V_{GS}=10V, I_{DS}=5A	12	21	30	nC
Q_{gs}	Gate-Source Charge		3.4	4.9	6.4	
Q_{gd}	Gate-Drain Charge		2.9	5.8	8.7	

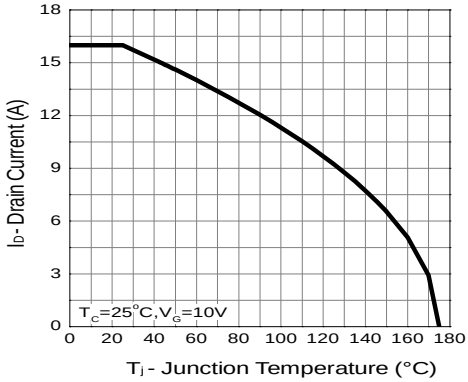
Note a : Pulse test ; pulse width≤300μs, duty cycle≤2%.
Note b : Guaranteed by design, not subject to production testing.

■ *TYPICAL CHARACTERISTICS (25℃ Unless Note)*

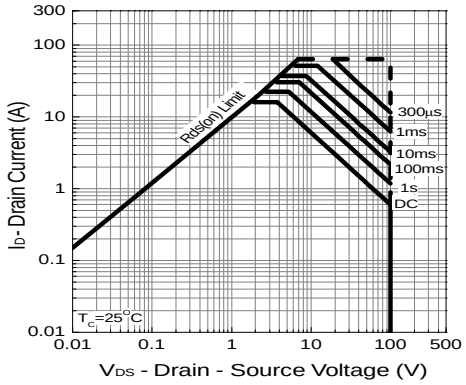
Power Dissipation



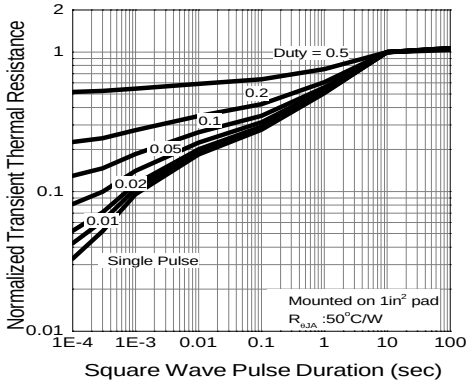
Drain Current



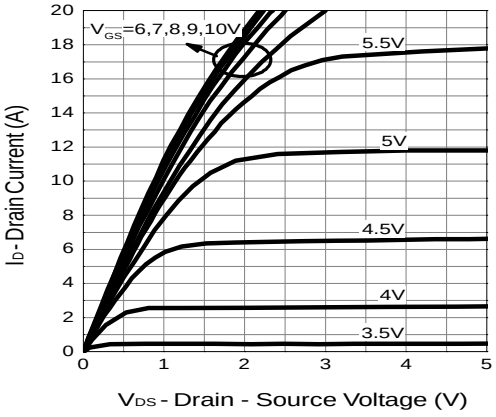
Safe Operation Area



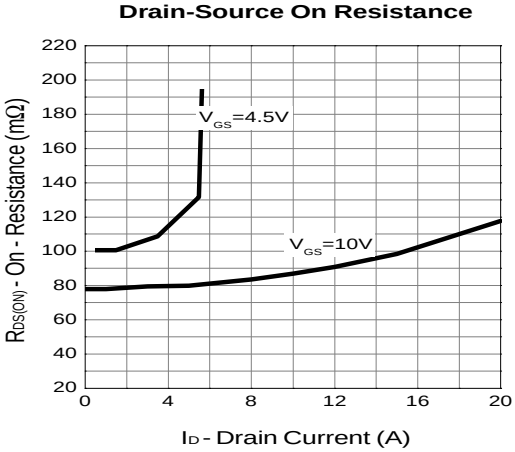
Thermal Transient Impedance



Output Characteristics

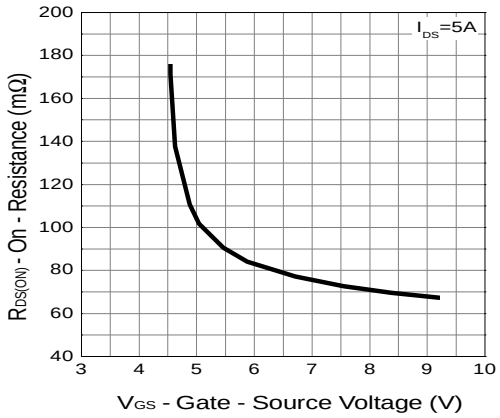


Drain-Source On Resistance

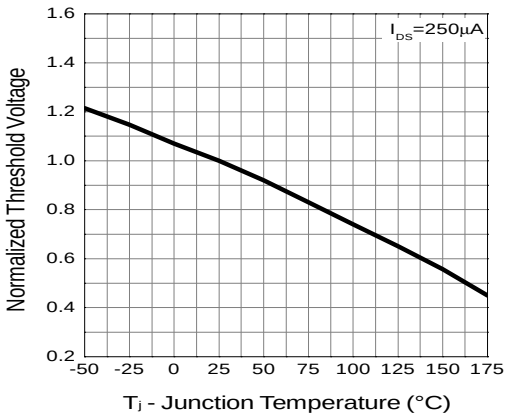


■ *TYPICAL CHARACTERISTICS (continuous)*

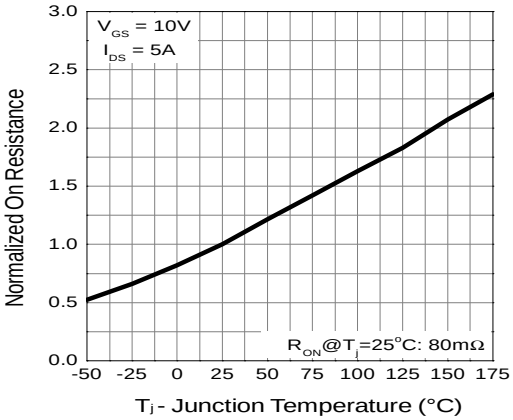
Gate-Source On Resistance



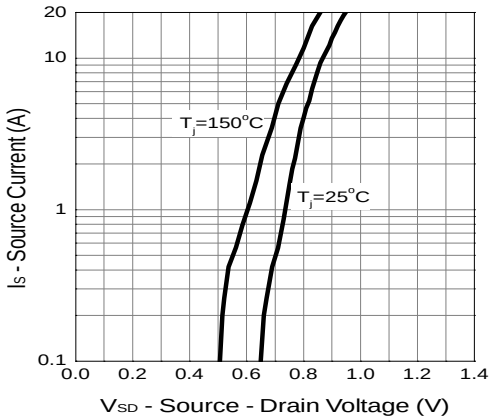
Gate Threshold Voltage



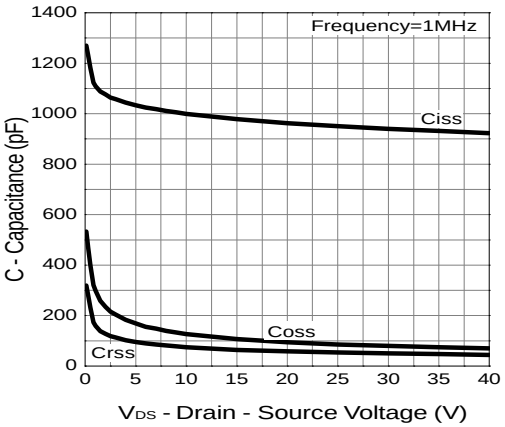
Drain-Source On Resistance



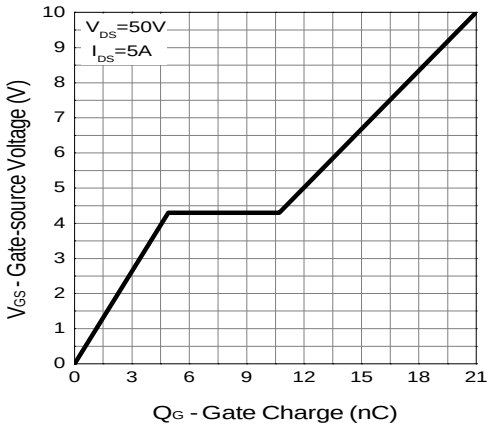
Source-Drain Diode Forward



Capacitance

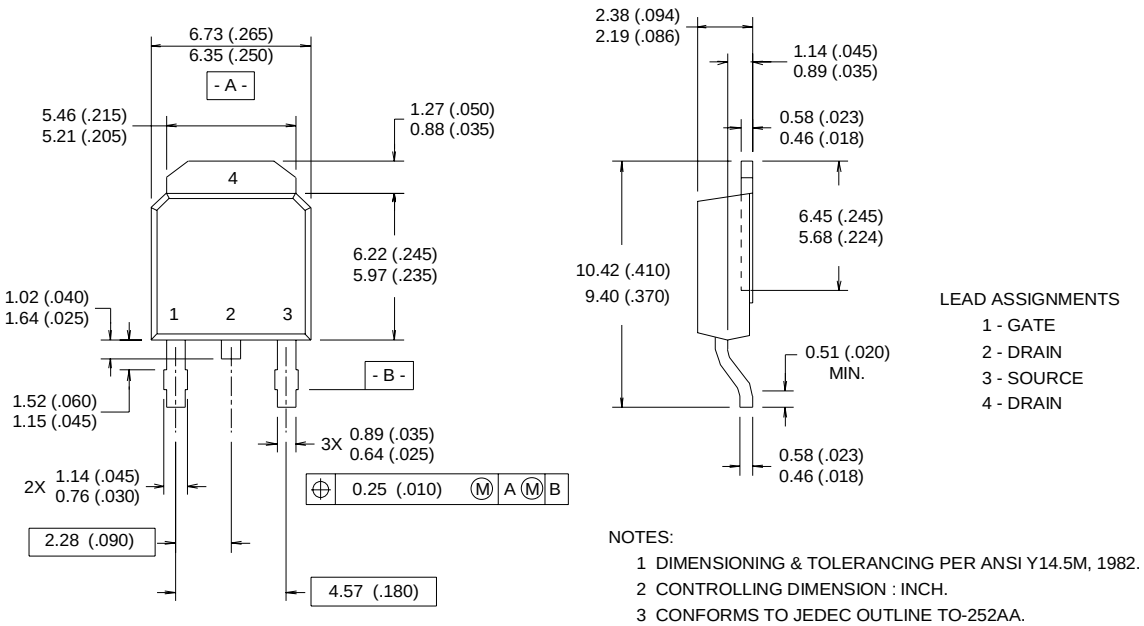


Gate Charge



■ TO-252 Outline Package Dimension

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

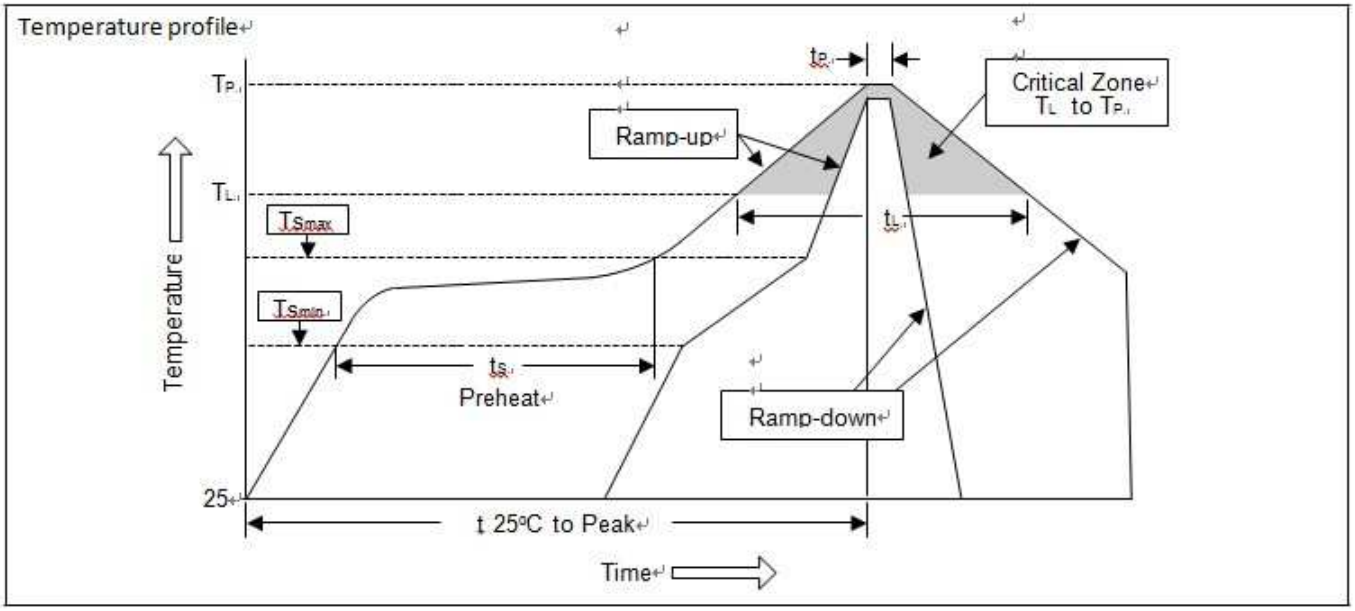
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

■ *SOLDERING METHODS FOR UNIVERCHIP*

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3℃/sec	<3℃/sec
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	 100℃ 150℃ 60~120 sec	 150℃ 200℃ 60~180 sec
Tsmax to T_L -Ramp-up Rate	<3℃/sec	<3℃/sec
Time maintained above -Temperature (T_L) -Time (t_L)	 183℃ 60~150 sec	 217℃ 60~150 sec
Peak Temperature (T_P)	240℃+0/-5℃	260℃+0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6℃/sec	<6℃/sec
Time 25℃ to Peak Temperature	<6 minutes	<6 minutes

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.